Application Note: AN-2301Q

Title	**SCALE EV B_OUT Readout: Signal Filter Guidelines**
Application	Bit Stream Readout for “SCALE EV”
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1 Scope

This document shall cover the following topics:

1. Bit Stream Signal (B_OUT) Hardware Filter
2. NTC Software Filter

These filters are recommended when using the SCALE EV products containing SCALE-iDriver2 IC SIC2192FQ or similar IC products with BitStream technology, in applications with electrically noisy environments, such as inverters or switched-mode power converters. Without mitigation measures, high noise levels can couple into the communication loop, which could result in erroneous results. This document outlines suggested methods to keep signal-to-noise levels within acceptable limits to ensure accurate readings from the bitstream signal.

2 Introduction

SCALE EV features a failure and status monitoring via a bit stream <B_OUT>, containing status and measurement data, plus a dedicated fault pin <SO>. The <SO> pin can be used as an interrupt trigger, ensuring the status is read and immediately addressed by the system.

The <B_OUT> signal is a fixed-frequency pulse train with a nominal frequency of 400 kHz. Information is encoded in the signal’s duty cycle, as defined in Figure 1.

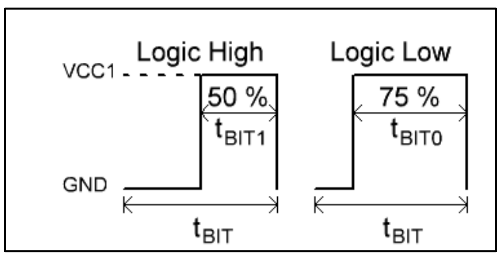

Figure 1. Logic Low and High Bit

The <B_OUT> is a push-pull 0V - 5V output that periodically transmits data in frames which consists of a Start Bit (Logic High), 27 Payload bits and 1 Stop bit. Before the Start Bit, a series of Logic Low bits (B_OUT[idle]) are sent as a preamble. The number of idle bits is not fixed and is defined by the asynchronous frame time t_{B_OUT} minus the time required for transmitting the Start Bit, Pay Load bits and the Stop Bit.

Idle Bits	**B_OUT Frame**			
	Start Bit	Pay Load Word		Stop Bit
		A / D Temperature Signal	Diagnostic and Monitoring Information	
B_OUT[idle]	B_OUT[1]	B_OUT[2:13]	B_OUT[14:28]	B_OUT[29]

A sample B_OUT frame is shown in the oscilloscope snapshot in Figure 2.

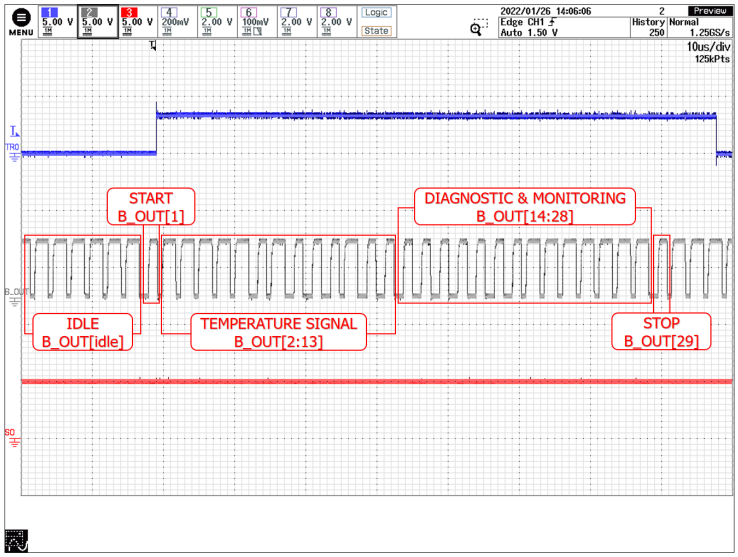

Figure 2. Oscilloscope Snapshot of a B_OUT Frame

Ideally, the microcontroller that receives the B_OUT signal must be placed as close as possible to the SCALE-EV board to maintain signal integrity. Unfortunately, it is more common in high-power applications to have the gate drivers and the microcontrollers on separate boards, which are then connected using a cable. This kind of setup can introduce noise coming from differential mode current through the wiring. With the 400 kHz switching frequency of B_OUT, the effects of this parasitic may become significant such that the signal can be distorted. Since the differentiation between bit ‘0’ and ‘1’ is define by the pulse width, a change on the shape of the signal may lead to false information received.

Aside from wiring parasitic, common mode current and magnetic field coupling can also introduce noise into the system as a result of high dv/dt and di/dt happening across the power semiconductor. All these sources of noise are illustrated on Figure 3 below.

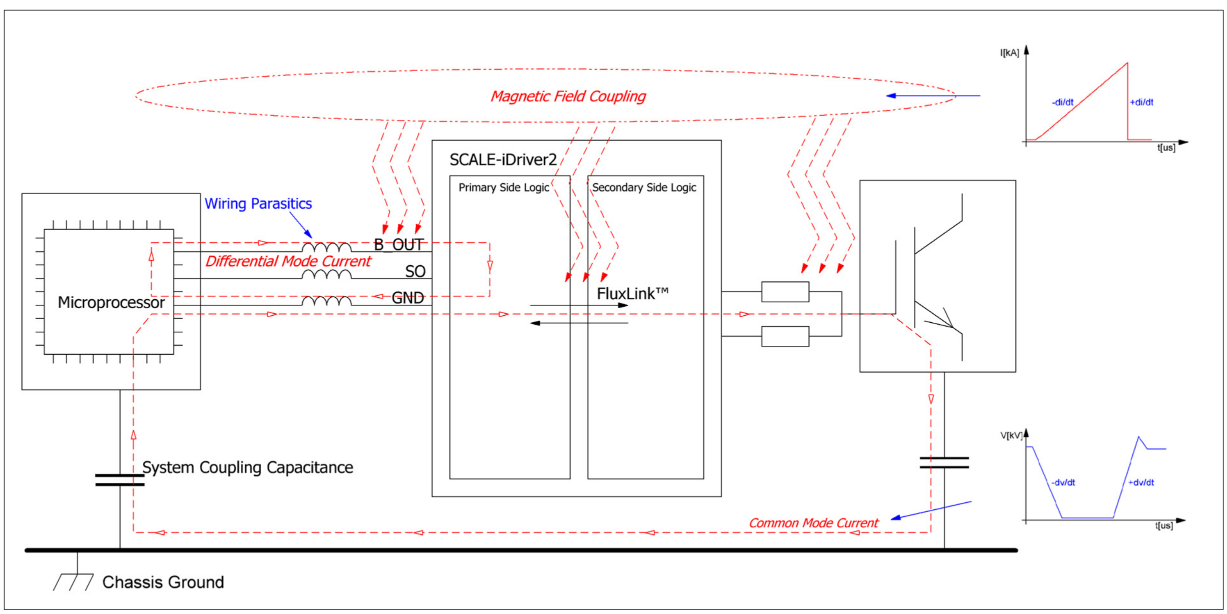

Figure 3. Sources of Noise

These noises influence the communication loops both internally (primary to secondary, v.v.) and externally (microprocessor to gate driver, v.v.). For internal communication, the SCALE EV features a robust transmission channel via SCALE-iDriver2 called FluxLink™. Information can still be successfully transferred even if parts of the data is corrupted under fast switching dv/dt and di/dt environments. However, for external communication, additional steps are recommended to achieve better noise immunity.

3 B_OUT Hardware Filter

A way to improve the signal integrity between the microprocessor and gate driver is via a hardware filter. Figure 4 shows a recommended filter implementation. The value of the impedances was based on actual test and evaluation during an inverter operation.

Any noise present on the B_OUT signal will be filtered through this circuit prior data processing by the microprocessor. Thus, it is important to place this filter as close as possible to the microprocessor pin.

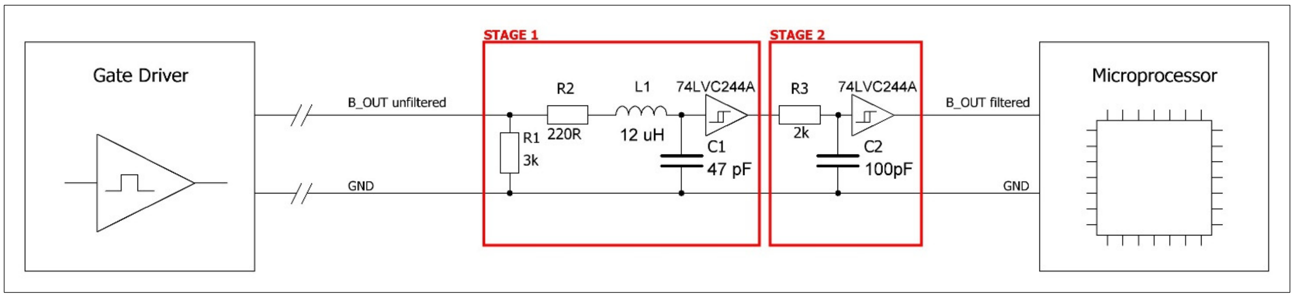

Figure 4. B_OUT Hardware Filter

This hardware filter is a two-stage Schmitt trigger buffers with pre-analog filter. Stage 1 is intended for filtering out extremely high frequency signals (noise), whereas stage 2 is for filtering out false impulses (glitch). The Schmitt-Trigger buffer provides input hysteresis to prevent erratic outputs due to input oscillations.

Stage 1 can be analyzed as an 2nd order RLC low pass filter, with R2 being the resistance, L1 as the inductance and C1 as the capacitance.

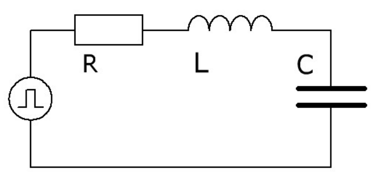

Figure 5. 2nd order RLC low pass filter

The transfer function of this filter is computed as:

$$\frac{V_{out}}{V_{in}} = \frac{1}{j2\pi f RC - (2\pi f)^2 LC + 1}$$

The cutoff frequency is calculated as the point at which the magnitude gain is equal to $^1/_{\sqrt{2}}$

$$\left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\sqrt{2}}$$

Combining both equations and solving for f_c yields to:

$$f_c = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{R^2}{2L^2} + \sqrt{\frac{R^4}{4L^4} - \frac{R^2}{L^3 C} + \frac{2}{L^2 C^2}}}$$

Substituting the recommended values of R = 220 Ω, L = 12 µH and C = 47 pF gives a cut-off frequency of 10 MHz. This was confirmed with the simulation shown in Figure 6.

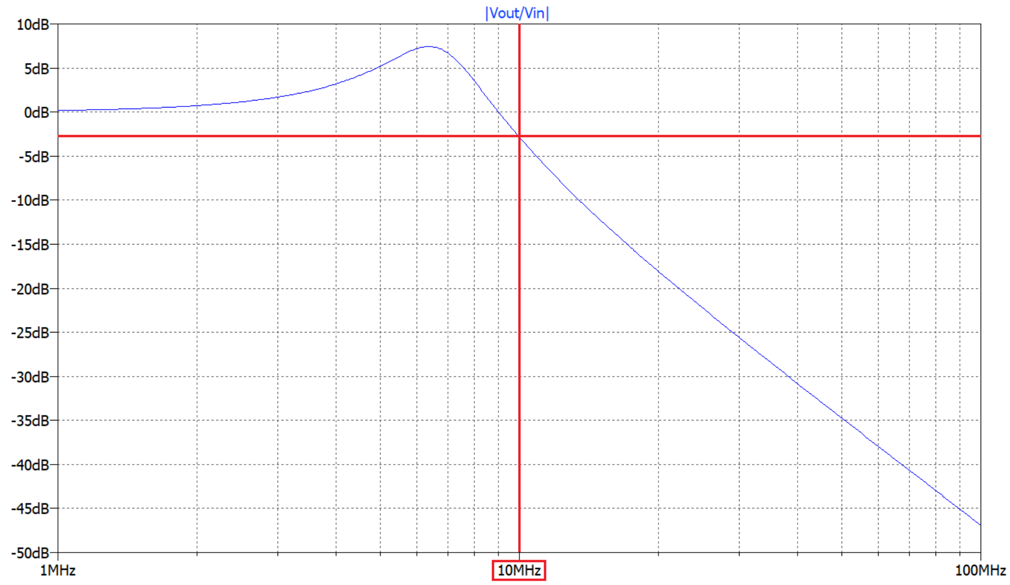

Figure 6. Simulation of RLC Filter

With this cut-off frequency, extremely high frequency noise will be filtered out without any alteration on the 400 kHz square-wave signal of the B_OUT data.

As for the stage 2, this can be analyzed as a simple RC low pass filter, with R3 being the resistance and C2 as the capacitance.

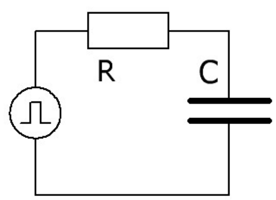

Figure 7. RC Low Pass Filter

Since this filter is intended for signal de-glitch, the smallest pulse width on the true signal needs to be defined first. As shown in Figure 8, the smallest pulse in a B_OUT signal will occur during the off-time of logic low bit ’0’. This means that any pulse width much less than this off-time is considered a false pulse or a glitch.

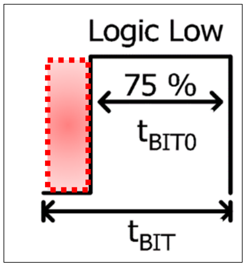

Figure 8. Logic Low of B_OUT

Using datasheet values, the length of this off-time pulse can be computed as follows:

$$Shortest\ Pulse\ Width = t_{BIT,min}\left(1 - t_{BIT0,max}\right) = 2.25\ \mu s\ (1 - 0.74) = \mathbf{585\ ns}$$

To provide enough margin between a glitch and a true signal, the RC network was arbitrarily set to treat a pulse as a glitch if its width is less than the third of 585 ns. As such, the value of the RC network is computed as follows:

$$\tau = R * C = {}^{585\ ns}/_{3}$$

Choosing a capacitance of 100 pF, the resistance is computed as follows:

$$R = \frac{195\ ns}{100\ pF} \sim 2\ k\Omega$$

4 NTC Software Filter

Included in the B_OUT data is a temperature 12-bit data reading of any NTC thermistor. Shown in Figure 9 is an actual NTC measurement during an inverter simulation using Power Integrations' 2SP0215F2Q0C assembled on FF900R12ME7_B11. On average, the NTC resistance measurement is approximately 7 kΩ. However, there are erroneous measurement interpreted as high as 22 kΩ. These readings were deemed to be noise due to capacitive coupling between NTC and IGBT-Chips inside the power module.

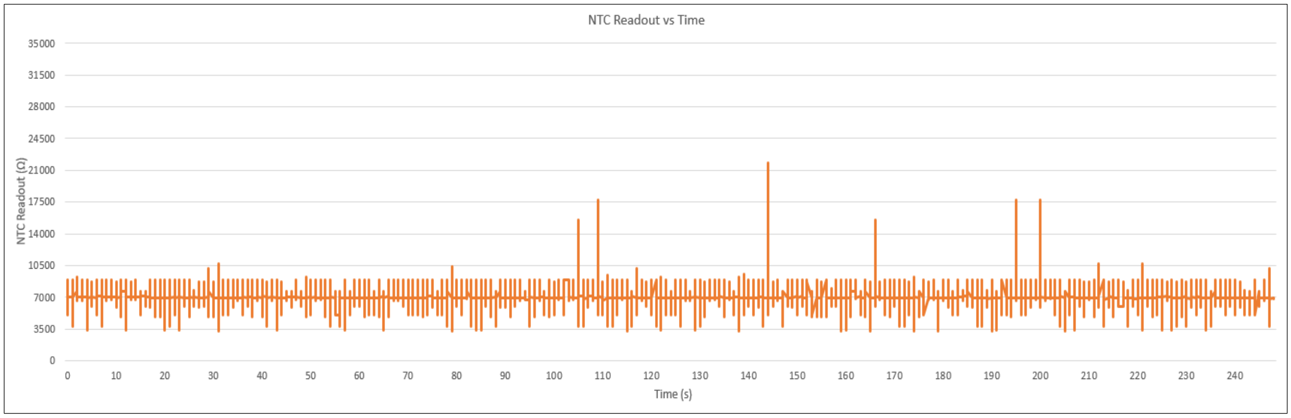

Figure 9. NTC Readout vs Time during Inverter Operation

The use of a filter capacitor in parallel with the NTC thermistor is not recommended because this is incompatible with the temperature sensing method of SCALE EV. As shown in Figure 10, adding a 10 nF capacitor in parallel with the NTC thermistor helps to flatten out the spikes, but the average reading was increased to around 32 kΩ which is way beyond the true reading.

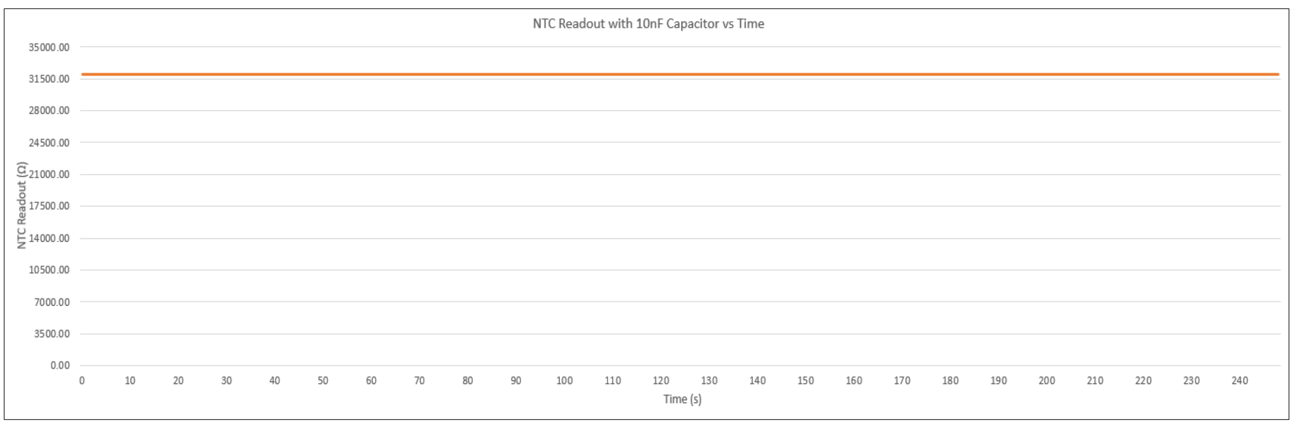

Figure 10. NTC Readout vs Time during Inverter Operation with 10nF Capacitor in Parallel

It is recommended to use a software statistical filter instead of a hardware-based solution. Shown in Figure 11 is a recommended software filter. The program simply adds or subtracts a fix delta (Δ) depending if the latest reading is greater or less than the active tempertature reading.

```
float act_Temp = NTC_Read(B_OUT);
float delta = 0.1;

float software_filter() {
    if (NTC_Read(B_OUT) > act_Temp)
        act_Temp += delta;
    else
        act_Temp -= delta;

    return act_Temp;
}
```

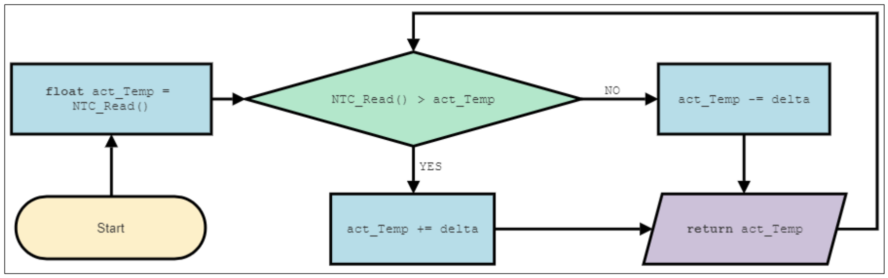

Figure 11. NTC Read-out Software Filter

Using the proposed software statistical filter on the measurements in Figure 9 yields a cleaner data with the correct average temperature as shown in Figure 12.

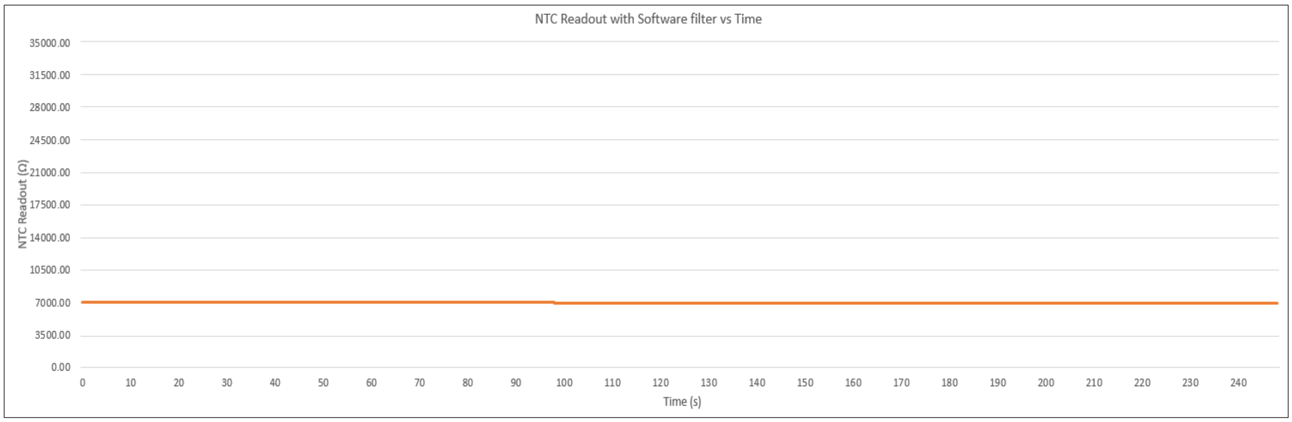

Figure 12. NTC Readout vs Time during Inverter Operation with Software Filter

The delta (Δ) used in this software filter was set to 0.1. Note that the value of (Δ) will directly limit the maximum rate of change in the NTC resistance measurement. This can be calculated as follows:

$$Rate\ of\ Change\ per\ second = (no. of\ NTC\ measurement\ samples\ per\ second) * (\Delta)$$

Given that the temperature sampling time of the SCALE EV is around 5 ms:

$$Rate\ of\ Change\ per\ second = \frac{1\ sample}{0.005\ s}(1\ s)(\Delta) = 200(\Delta)\ {}^{\Omega}/_{s}$$

Depending on the sensitivity required of the application, the value of (Δ) could be changed accordingly.

Figure 13 shows the effect of different delta. The higher the delta value, the faster the response will be, but there will be a draw back on data precision.

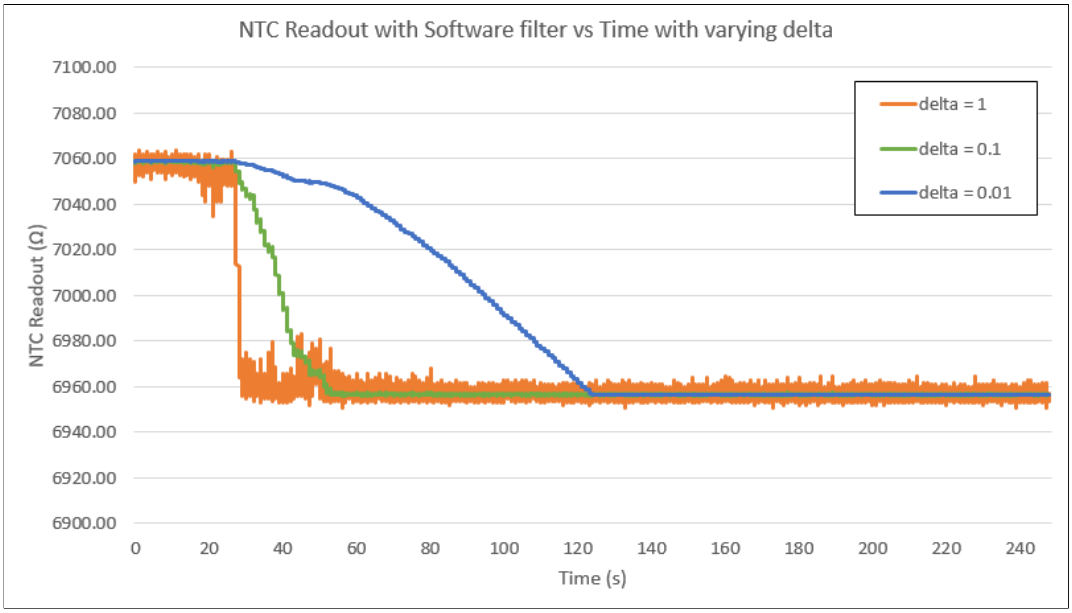

Figure 13. NTC Readout vs Time across different Delta

The heatsink of a power semiconductor module or even an external NTC on PCB provides a large thermal capacity. With this thermal capacity, fast temperature changes are not possible. Therefore, a filter time with delta < 0.1 is recommended for this software filter.

5 Revision History

Date	Author	Revision	Description and changes	Reviewed
20-Mar-23	CO	1.0	Initial Release.	MH

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