Design Example Report

Title	***3-Phase Inverter Using BridgeSwitch™ BRD1265C***
Specification	270 VDC – 365 VDC Input; 300 W Inverter Output, 1.0 A Motor RMS Current
Application	High-Voltage Brushless DC (BLDC) Motor Drive
Author	Applications Engineering Department
Document No.	DER-654
Date	May 20, 2019
Revision	1.1

Summary and Features

- BridgeSwitch – high-voltage half-bridge motor driver
  - Integrated 600 V FREDFETs with ultra-soft, fast recovery diodes
- Fully self-biased operation – no auxiliary power supply needed
- No external heat sink
- Instantaneous phase current output signal
- High-side and low-side cycle-by-cycle current limit
- Two level device over-temperature protection
- High-voltage bus monitor with four undervoltage threshold and one overvoltage threshold
- System level temperature monitor
- Single wire status update communication bus
- Supports trapezoidal and sinusoidal commutation

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Table of Contents

Important Note:
During operation, the design example board is subject to hazards including high voltages, rotating parts, bare wires, and hot surfaces. Energized DC bus capacitors require time to discharge after DC input disconnection.

All testing should use an isolation transformer to provide the DC input to the board.

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1 Introduction

This document is an engineering report describing a 300 W, >98% efficiency 3-phase inverter for a high-voltage brushless DC (BLDC) motor drive using three BridgeSwitch BRD1265C devices. This design shows the device performance, internal and system level monitoring and fault protection facilitated by the high level of integration of the BridgeSwitch half-bridge motor driver IC.

This document contains the inverter specification, schematic, bill of materials, printed circuit board layout, and test setup. Provided waveform plots and performance data employed a traditional six-step trapezoidal BLDC motor control scheme. The design can also operate with other control methods such as sinusoidal commutation.

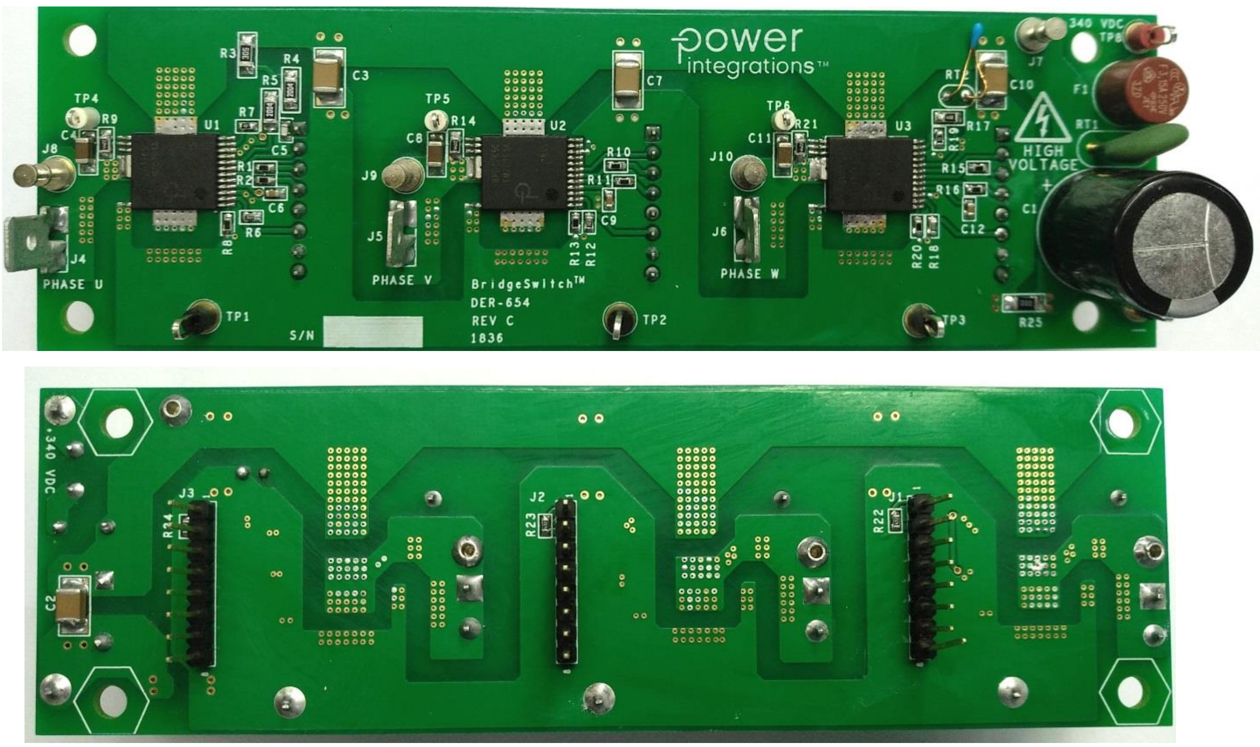

Figure 1 – Populated Circuit Board Photograph Top and Bottom View.

2 Inverter Specification

The table below provides the electrical specification of the 3-phase inverter design. The results section provides actual performance data.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	270	340	365	V	2-Wire High-Voltage DC Bus
Power	P_{IN}		305		W	
Output						
Power	P_{OUT}		300		W	Inverter Output
Motor Current	I_{MOTOR}		1.0		A	RMS
PWM Carrier Frequency[1]	f_{PWM}		12	20	kHz	Self-Supplied Operation
Efficiency						
Full Load			98.0		%	300 W Output, Motor at 5000 RPM.
Environmental						
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection.
System Level Monitoring						Reported Through Status Communication Bus.
DC Bus Sensing						
OV Threshold	V_{OV}		422		V	
1st UV Threshold	V_{UV100}		247		V	
2nd UV Threshold	V_{UV85}		212		V	
3rd UV Threshold	V_{UV60}		177		V	
4th UV Threshold	V_{UV55}		142		V	
Temperature Sense						
System Warning Temperature[2]	T_{SYS}		90		°C	

Notes: 1. 20 kHz is the maximum recommended PWM frequency with self-supply or with external supply.
2. Sensed through an external thermistor, temperature threshold depends on chosen NTC and its location, requires verification in final application.

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3 Schematic

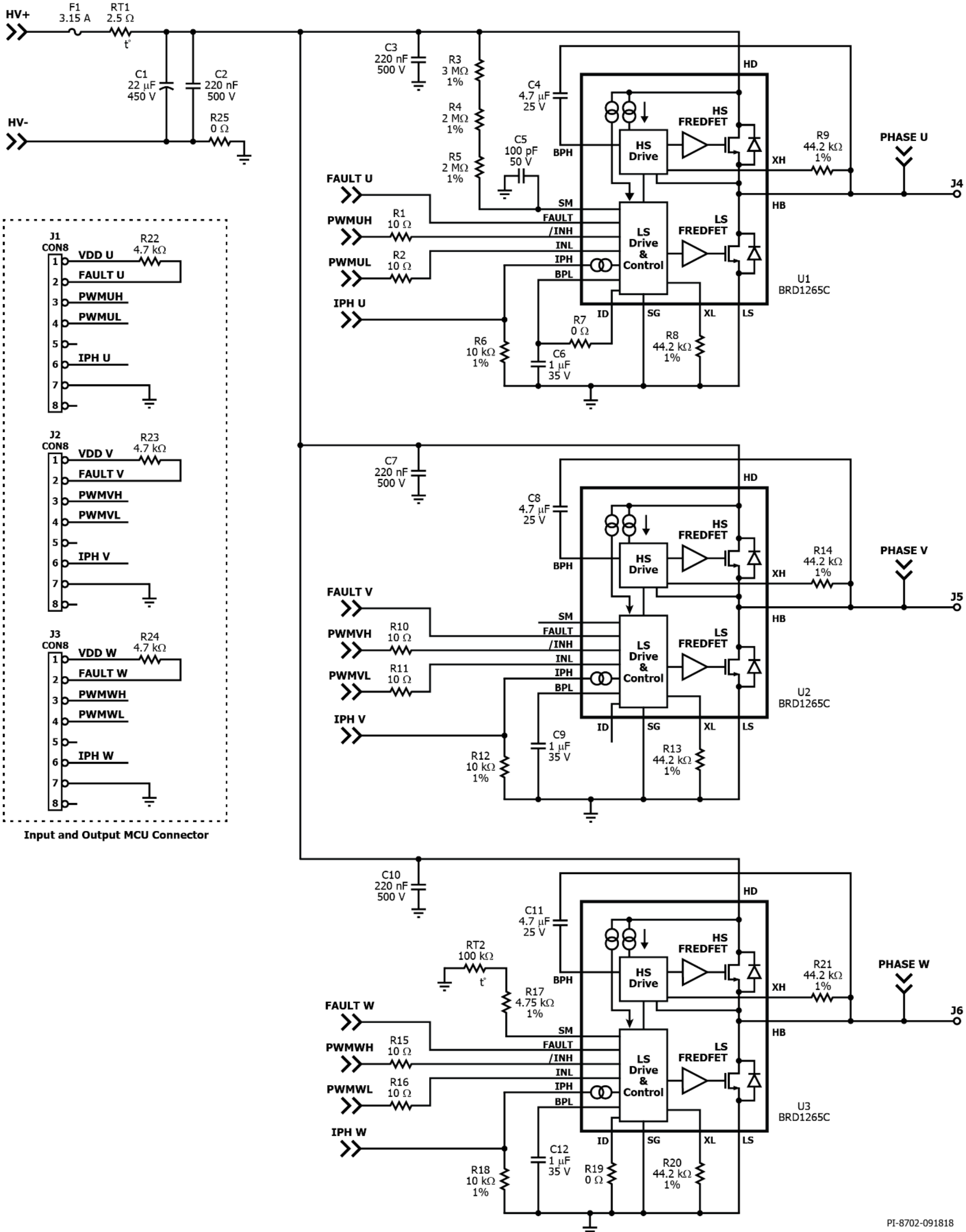

Figure 2 – BridgeSwitch 3-Phase Inverter Power Stage Schematic.

4 Circuit Description

The schematic in Figure 2 shows a 3-phase inverter employing three BRD1265C devices. The circuit enables driving a high-voltage, 3-phase brushless DC (BLDC) motor from a rectified AC input voltage. It supports various motor control schemes such as trapezoidal or sinusoidal commutation. Major and comfort appliances commonly use this type of motor because of its increased efficiency and reduced audible noise. BridgeSwitch combines two N-channel 600 V rated power FREDFETs, gate drivers and controllers into a low profile surface mount package. The power FREDFETs feature ultra-soft, fast recovery diodes ideally suited for hard switched inverter drives. Both drivers are fully self-supplied eliminating the need for an external power supply for the design. BridgeSwitch has device internal fault protection and system-level monitoring. Internal fault protection includes cycle-by-cycle current limit for both FREDFETs and two-level thermal overload protection. System level monitoring includes high-voltage DC bus sensing with multi-level under-voltage thresholds and one over-voltage threshold as well as driving external sensors such as a thermistor for system temperature monitoring. A single-wire open-drain bus communicates all detected fault or status change conditions to the system microcontroller. The inverter board does not have heat sinks.

4.1 Input stage

The input stage provides local decoupling of the rectified AC mains through capacitors C1 and C2. Fuse F1 provides over-current protection and thermistor RT1 limits the inrush current. Resistor R25 allows optional sensing of the input DC return current.

4.2 3-Phase BridgeSwitch Inverter

The three BridgeSwitch devices U1, U2, and U3 form the 3-phase inverter. The outputs of the inverter connect to the 3-phase BLDC motor through connectors J4, J5, and J6.

4.2.1 *Self-Supply Operation*

Capacitors C6, C9, and C12 provide self-supply decoupling for the integrated low-side controller and gate driver. Internal high-voltage current sources recharge them as soon as the voltage level starts to dip. Capacitors C4, C8, and C11 provide self-supply decoupling for the integrated high-side controller and gate driver. Internal high-voltage current sources recharge them whenever the half-bridge point of the respective device drops to the low-side Source voltage level (i.e. the low-side FREDFET turns on).

4.2.2 *PWM Input*

Input signals PWMUH, PWMUL, PWMVH, PWMVL, PWMWH, and PWMWL control the switching state of the integrated high side and low side power FREDFETs. The system microcontroller can access the PWM inputs through pins 3 and 4 of the connectors J1, J2, and J3. Refer to section 8.1.1 for more details.

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4.2.3 *Local Decoupling Capacitors*

Capacitors C3, C7, and C10 provide decoupling of the high-voltage DC bus local to BridgeSwitch devices U1, U2, and U3.

4.2.4 *Cycle-by-Cycle Current Limit*

Resistors R8, R9, R13, R14, R20, and R21 set the cycle-by-cycle current limit level for the integrated low-side and high-side power FREDFETs. The selected value of 44.2 kΩ sets it to 100% of the default level or 3 A.

4.2.5 *Instantaneous Phase Current Information*

Each BRD1265C provides instantaneous phase current information through its IPH output across resistors R6, R12, and R18. The IPH pin output gain is 100 μA/A, which translates into a 1 V signal for a 1 A Drain current with the selected value of 10 kΩ. The voltage signal is available on pin 6 of connectors J1, J2, and J3.

4.2.6 *System Undervoltage and Overvoltage Monitoring and Protection*

BridgeSwitch U1 monitors the DC bus voltage through resistors R3, R4, and R5. Their combined resistance of 7 MΩ sets the under-voltage thresholds to 247 V, 212 V, 177 V, and 142 V. The set bus over-voltage threshold is 422 V. Capacitor C5 provides high frequency noise decoupling at the SM-pin. The FAULT-pin reports any detected bus voltage fault condition to the system MCU via the communication bus.

4.2.7 *System-Level Temperature Monitoring*

BridgeSwitch U3 monitors the system temperature through thermistor RT2 connected to its SM-pin. Resistor R17 tunes the threshold for a system level fault of 90 °C.

4.2.8 *Fault Communication*

The devices will report any detected internal and system fault through the communication bus located on pin 2 of connectors J1, J2, and J3 with each FAULT pin pulled-up to VDD via R22, R23 and R24. All three FAULT pins can be tied together in a single wire bus using only one pull-up resistor (4.7 kΩ) to VDD. In this case, R23 and R24 should be depopulated.

4.2.9 *Device ID*

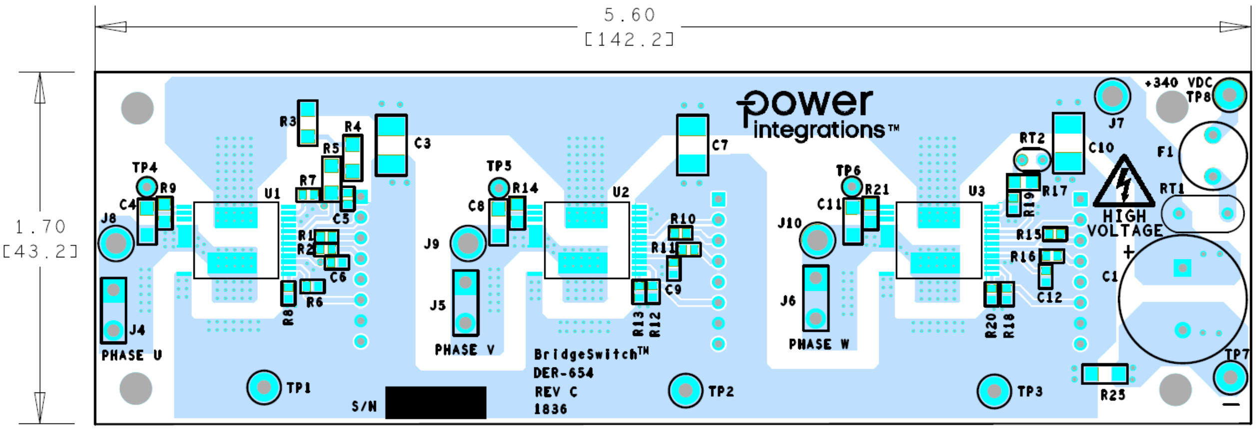
Each BRD1265C assigns itself a unique device ID by configuring its ID pin connection: device U1 ID pin connected to BPL pin via R7 (40 μS t_{ID}), device U2 ID pin floating (60 μS t_{ID}), and device U3 ID pin shorted to SG via R19 (80 μS t_{ID}). The device ID supports FAULT bus arbitration and enables communicating the physical location of a detected fault to the system microcontroller.

4.2.10 *Microcontroller Interface*

Connectors J1, J2, and J3 interface the three-phase inverter stage to the system microcontroller for the PWM input, IPH output and fault output signals. VDDU, VDDV, and VDDW provide the pull-up supply for the open-drain fault output.

5 Printed Circuit Board Layout

Top View



Bottom View

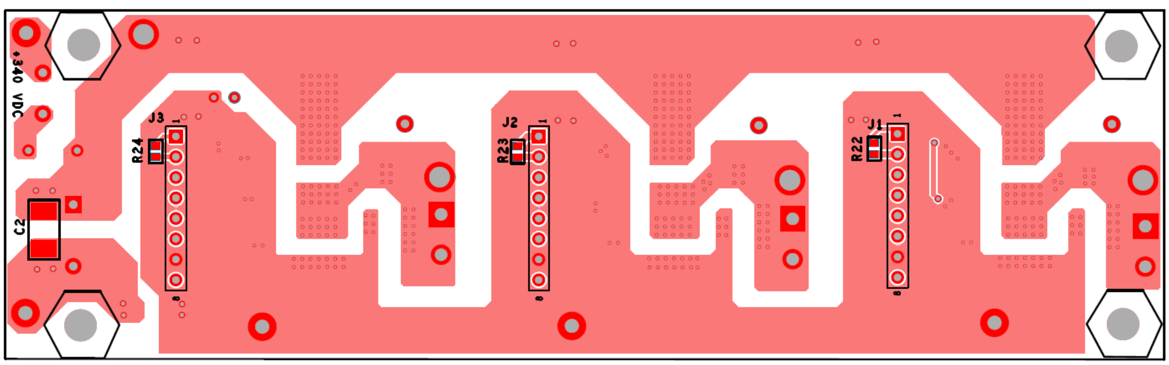


Figure 3 – Printed Circuit Board Layout Top and Bottom View.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C1	22 μF, ±20%, 450 V, Aluminum, Radial	EEU-ED2W220S	Panasonic
2	4	C2, C3, C7, C10	220 nF, 500 V, Ceramic, X7R, 1812	C1812C224KCRACTU	Kemet
3	3	C4, C8, C11	4.7 μF, 50 V, Ceramic, X7R, 1206	GCM31CR71E475KA55L	Murata
4	1	C5	100 pF, 50 V, Ceramic, NP0, 0603	CC0603JRNPO9BN101	Yageo
5	3	C6, C9, C12	1 μF, 35 V, ±10% Ceramic, X7R, 0603	CGA3E1X7R1V105K080AC	TDK
6	1	F1	3.15 A, 250 V, Slow, TR5	37213150411	Wickman
7	3	J1, J2, J3	8 Position (1 x 8) header, 0.1 pitch, 0.318"	PRPC008SFAN-RC	Sullins
8	3	J4, J5, J6	CONN QC TAB 0.250 SOLDER	1287-ST	KeyStone
9	4	J7, J8, J9, J10	Terminal, Turret Connector, Single End, 0.281"	1514-2	Keystone
10	4	POST-CRKT_BRD_6-32_HEX1, POST-CRKT_BRD_6-32_HEX2, POST-CRKT_BRD_6-32_HEX3, POST-CRKT_BRD_6-32_HEX4	Post, Circuit Board, Female, Hex, 6-32, snap, 0.375L, Nylon	561-0375A	Eagle Hardware
11	6	R1, R2, R10, R11, R15, R16	RES, 10 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
12	1	R3	RES, 3 MΩ, 1%, 1/4 W, Thick Film, 1206	KTR18EZPF3004	Rohm
13	2	R4, R5	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
14	3	R6, R12, R18	RES, 10 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1002V	Panasonic
15	2	R7, R19	RES, 0 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEY0R00V	Panasonic
16	3	R8, R13,R20	RES, 44.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4422V	Panasonic
17	3	R9, R14, R21	RES, 44.2 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4422V	Panasonic
18	1	R17	RES, 4.75 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4751V	Panasonic
19	3	R22, R23, R24	RES, 4.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
20	1	R25	RES, 0 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEY0R00V	Panasonic
21	1	RT1	NTC Thermistor, 2.5 Ω, 5 A	SCK102R55ALSY	Thinking Electronics Industrial
22	1	RT2	NTC Thermistor, 100 kΩ, 1%, 30 mm leads,-40 C to +125 C	NXFT15WF104FA1B030	Murata
23	4	TP1, TP2, TP3, TP7	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
24	3	TP4, TP5, TP6	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
25	1	TP8	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
26	3	U1, U2, U3	BridgeSwitch, Full Featured, Max. BLDC Motor Current 1.00A(RMS)	BRD1265C	Power Integrations

7 Performance Data

This section presents waveform plots and performance data gathered with the test bench described in section 8.3 The method used to measure the inverter output power is described in section 8.4

The HV bus voltage level is 340 VDC unless stated otherwise. Light-load measurements describe the inverter operating at 50 W input power. Full load operation describes the inverter operating at 305 W input power. All measurements were performed at room ambient temperature.

7.1 Start-up Operation

Figure 4 shows the low-side and high-side BYPASS pin voltages of device U3 (phase W) after HV bus turn-on. The start-up power-up sequence follows the recommended startup sequence described in section 8.1.3. The HV bus turn-on slew rate is set to 5 V / ms.

Figure 5 depicts motor start-up waveforms captured at phase W at light load.

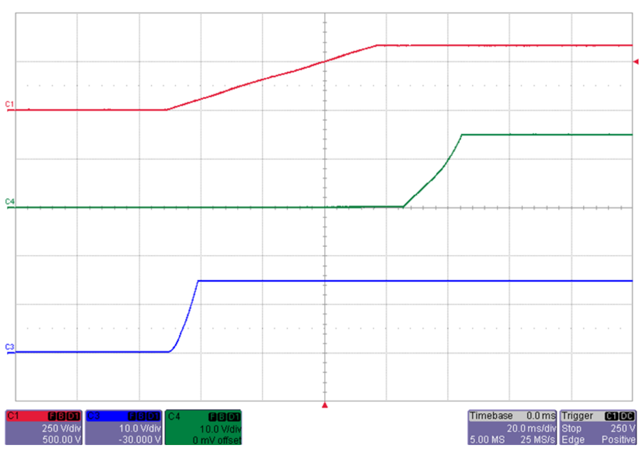

Figure 4 – Device Self-Supply Start-up.
Device U3, Phase W.
Upper: HV Bus, 250 V / div.
Middle: V_{BPH-HB}, 10 V / div.
Lower: V_{BPL}, 10 V / div.
Time Scale: 20 ms / div.

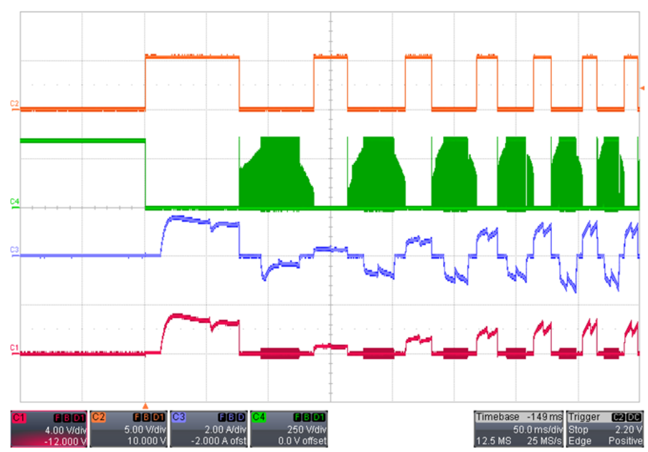

Figure 5 – Motor Start-up at Light Load.
First: INL Input, 5 V / div.
Second: V_{HB}, 250 V / div.
Third: $I_{PHASE\ W}$, 2 A / div.
Fourth: V_{IPH}, 4 V / div.
Time Scale: 50 ms / div.

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7.2 Steady-State Operation

Figure 6 to 9 depict the 3-phase half-bridge point voltage waveforms and phase currents.

7.2.1 *Phase Voltages During Steady-State*

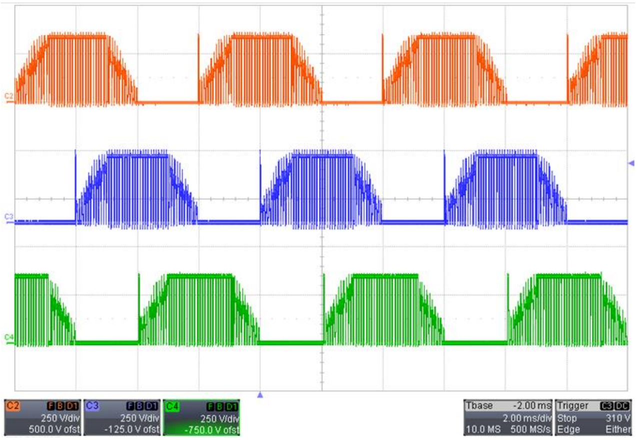

Figure 6 – Steady-State – 5000 RPM, Light Load.
Upper: $V_{HB(PHASE\ U)}$, 250 V / div.
Middle: $V_{HB(PHASE\ V)}$, 250 V / div.
Lower: $V_{HB(PHASE\ W)}$, 250 V / div.
Time Scale: 2 ms / div.

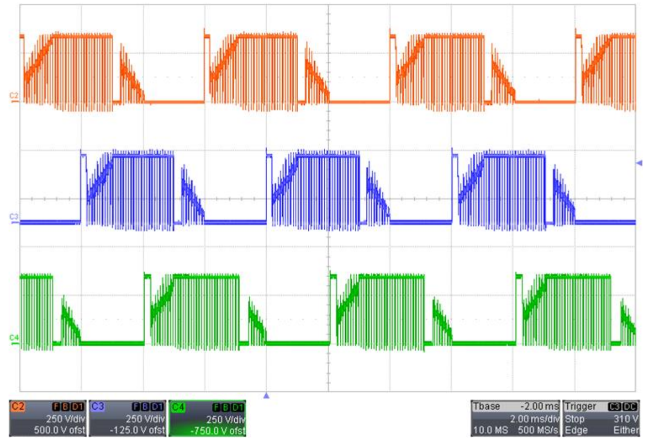

Figure 7 – Steady-State – 5000 RPM, Full Load.
Upper: $V_{HB(PHASE\ U)}$, 250 V / div.
Middle: $V_{HB(PHASE\ V)}$, 250 V / div.
Lower: $V_{HB(PHASE\ W)}$, 250 V / div.
Time Scale: 2 ms / div.

7.2.2 *Phase Currents During Steady-State*

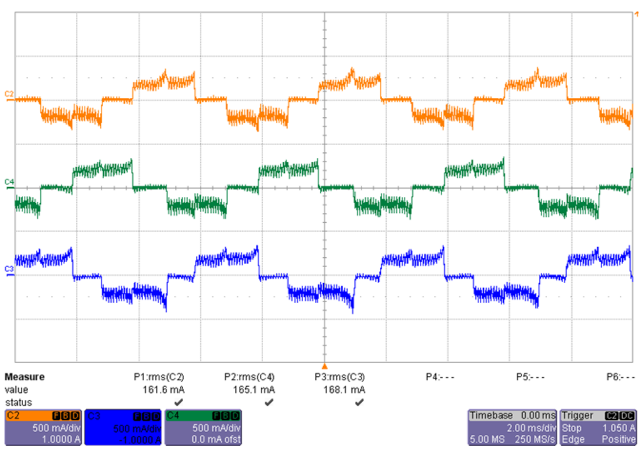

Figure 8 – Steady-State – 5000 RPM, Light Load.
$I_{MOTOR,\ RMS(U)}$: 161 mA.
$I_{MOTOR,\ RMS(V)}$: 165 mA.
$I_{MOTOR,\ RMS(W)}$: 168 mA.
Upper: $I_{MOTOR(U)}$, 500 mA / div.
Middle: $I_{MOTOR(V)}$, 500 mA / div.
Lower: $I_{MOTOR(W)}$, 500 mA / div.
Time Scale: 2 ms / div.

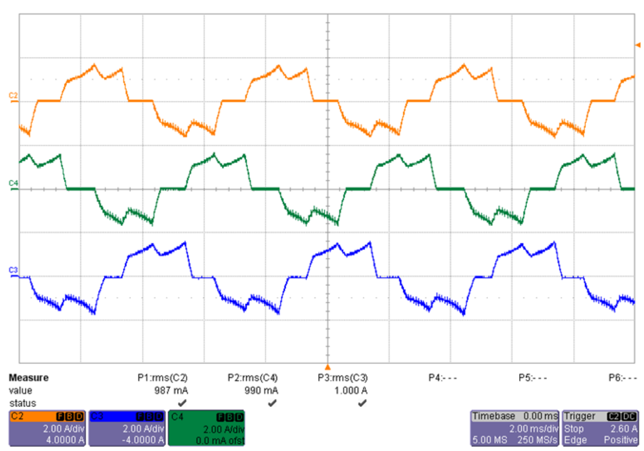

Figure 9 – Steady-State – 5000 RPM, full load.
$I_{MOTOR,\ RMS(U)}$: 0.98 A.
$I_{MOTOR,\ RMS(V)}$: 0.99 A.
$I_{MOTOR,\ RMS(W)}$: 1.0 A.
Upper: $I_{MOTOR(U)}$, 2 A / div.
Middle: $I_{MOTOR(V)}$, 2 A / div.
Lower: $I_{MOTOR(W)}$, 2 A / div.
Time Scale: 2 ms / div.

7.2.3 *Phase Current Information signal (IPH)*

Figure 10 to Figure 11 depict the 3-phase current waveforms and the corresponding phase current output signal (phase W) during light load and full load normal operation.

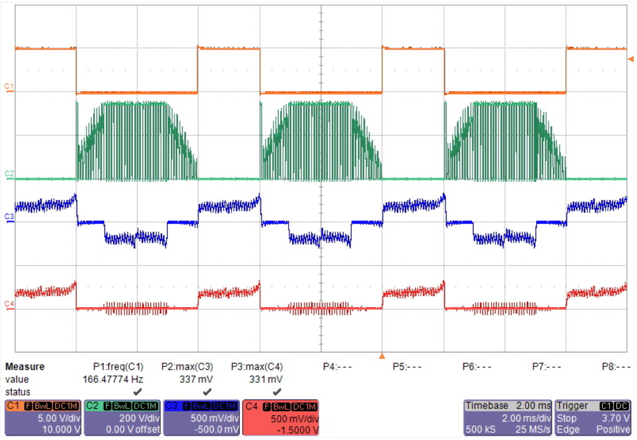

Figure 10 – Steady-State – 5000 RPM, Light Load.
INL frequency: 166 Hz.
$V_{IPH(PK)}$: 0.337 V.
$I_{MOTOR(PK)}$: 0.331 A.
First: INL Input, 5 V / div.
Second: V_{HB}, 200 V / div.
Third: $I_{PHASE\ W}$, 500 mA / div.
Fourth: V_{IPH}, 500 mV / div.
Time Scale: 2 ms / div.

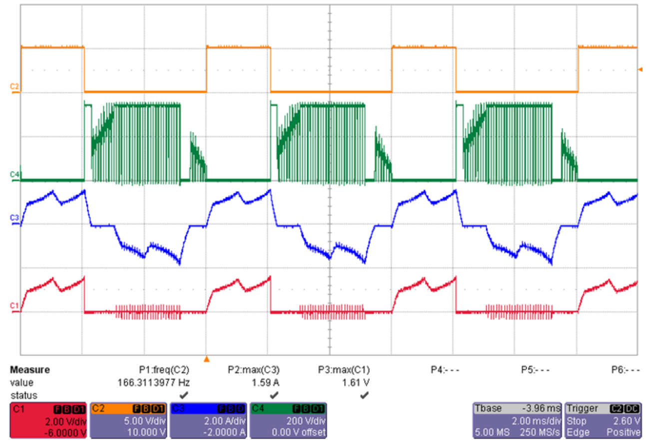

Figure 11 – Steady-State – 5000 RPM, Full Load.
INL Frequency: 166 Hz.
$V_{IPH(PK)}$: 1.61 V.
$I_{MOTOR(PK)}$: 1.59 A.
First: INL Input, 5 V / div.
Second: V_{HB}, 200 V / div.
Third: $I_{PHASE\ W}$, 2 A / div.
Fourth: V_{IPH}, 2 V / div.
Time Scale: 2 ms / div.

7.2.4 */INH and INL Input Signals*

Figure 12 and Figure 13 depict the low-side (INL) and high-side (/INH) Input PWM signals on the phase W device.

Figure 12 – Steady-State – 5000 RPM, Light Load.
Upper: INL Input, 5 V / div.
Middle: V_{HB}, 250 V / div.
Lower: /INH Input, 5 V / div., 2 ms / div.
Zoom: 50 μs / div.

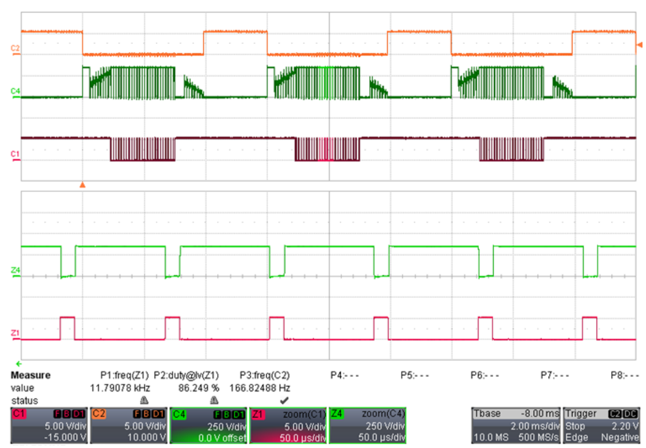

Figure 13 – Steady-State – 5000 RPM, Full Load.
Upper: INL Input, 5 V / div.
Middle: V_{HB}, 250 V / div.
Lower: /INH Input, 5 V / div., 2 ms / div.
Zoom: 50 μs / div.

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7.2.5 *Self-Supply BYPASS Pin Voltages During Steady-State*

Figure 14 and Figure 15 depict the low-side and high-side self-supply BYPASS pin voltages at steady state.

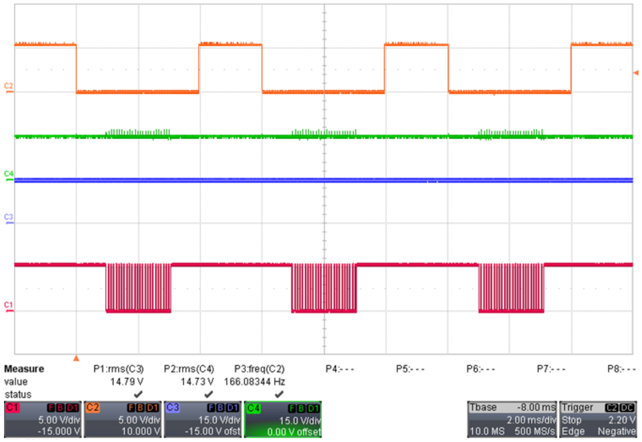


Figure 14 – Steady-State – 5000 RPM, Light Load.
Device: U3, Phase W.
First: INL Input, 5 V / div.
Second: V_{BPH-HB}, 15 V / div.
Third: V_{BPL}, 15 V / div.
Fourth: /INH Input, 5 V / div.
Time Scale: 2 ms / div.

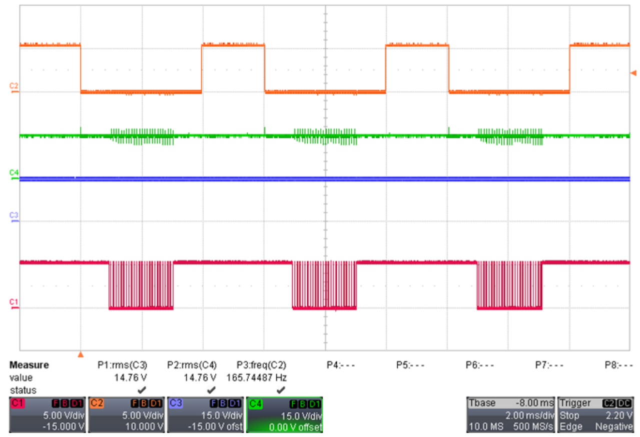


Figure 15 – Steady-State – 5000 RPM, Full Load.
Device: U3, Phase W.
First: INL Input, 5 V / div.
Second: V_{BPH-HB}, 15 V / div.
Third: V_{BPL}, 15 V / div.
Fourth: /INH Input, 5 V / div.
Time Scale: 2 ms / div.

7.2.6 *High-Side Drain Voltage Slew Rate at Full Load*

Figure 16 and Figure 17 depict high-side FREDFET Drain voltage slew rates at turn-on and turn-off, respectively.

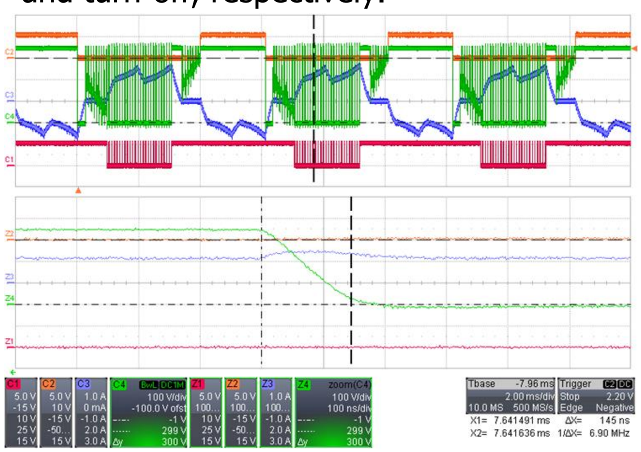


Figure 16 – Steady-State – 5000 RPM, Full Load.
High-Side FREDFET Turn-on.
Turn-On Voltage Slew Rate: 2.0 V / ns.
Upper: /INH Input, 5 V / div.
Middle: V_{HD-HB}, 100 V / div.
Lower: $I_{PHASE\ W}$, 1 A / div., 2 ms / div.
Zoom: 100 ns / div.

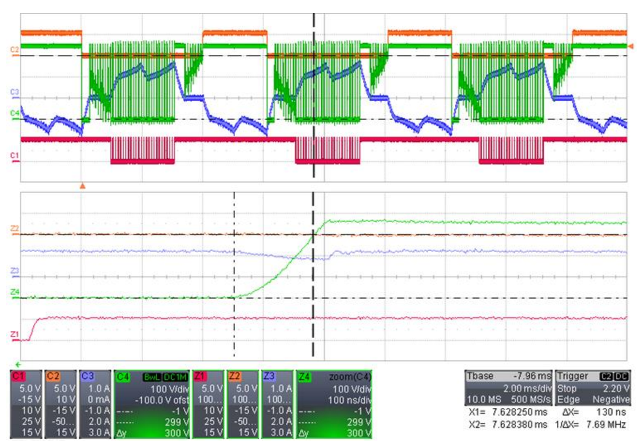
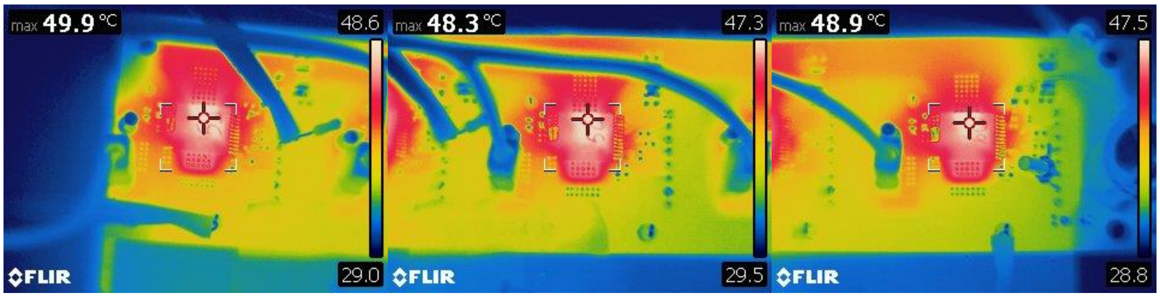


Figure 17 – Steady state – 5000 RPM, Full Load.
High-Side FREDFET Turn-Off.
Turn-Off Voltage Slew Rate: 2.3 V / ns.
Upper: /INH Input, 5 V / div.
Middle: V_{HD-HB}, 100 V / div.
Lower: $I_{PHASE\ W}$, 1 A / div., 2 ms / div.
Zoom: 100 ns / div.

7.3 Thermal Performance

Figure 18 depicts on-board device thermal scan after 30 minutes of operation for 100 W, 200 W and 300 W output power running a constant speed of 5000 RPM, with 12 kHz high-side PWM frequency at room ambient temperature.

7.3.1 *100 W*

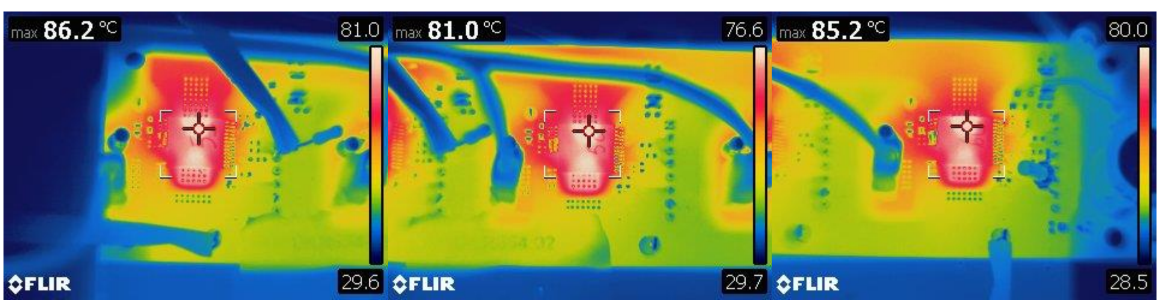


$I_{PHASE\ U(RMS)}$: 0.340 A	$I_{PHASE\ V(RMS)}$: 0.335 A	$I_{PHASE\ W(RMS)}$: 0.347 A

7.3.2 *200 W*

$I_{PHASE\ U(RMS)}$: 0.655 A	$I_{PHASE\ V(RMS)}$: 0.644 A	$I_{PHASE\ W(RMS)}$: 0.669 A

7.3.3 *300 W*



$I_{PHASE\ U(RMS)}$: 0.965 A	$I_{PHASE\ V(RMS)}$: 0.952 A	$I_{PHASE\ W(RMS)}$: 0.986 A

Figure 18 – Device Case Temperatures.

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7.4 No-Load Power Consumption

Figure 19 depicts the no-load input power consumption of the inverter measured across input line voltage.

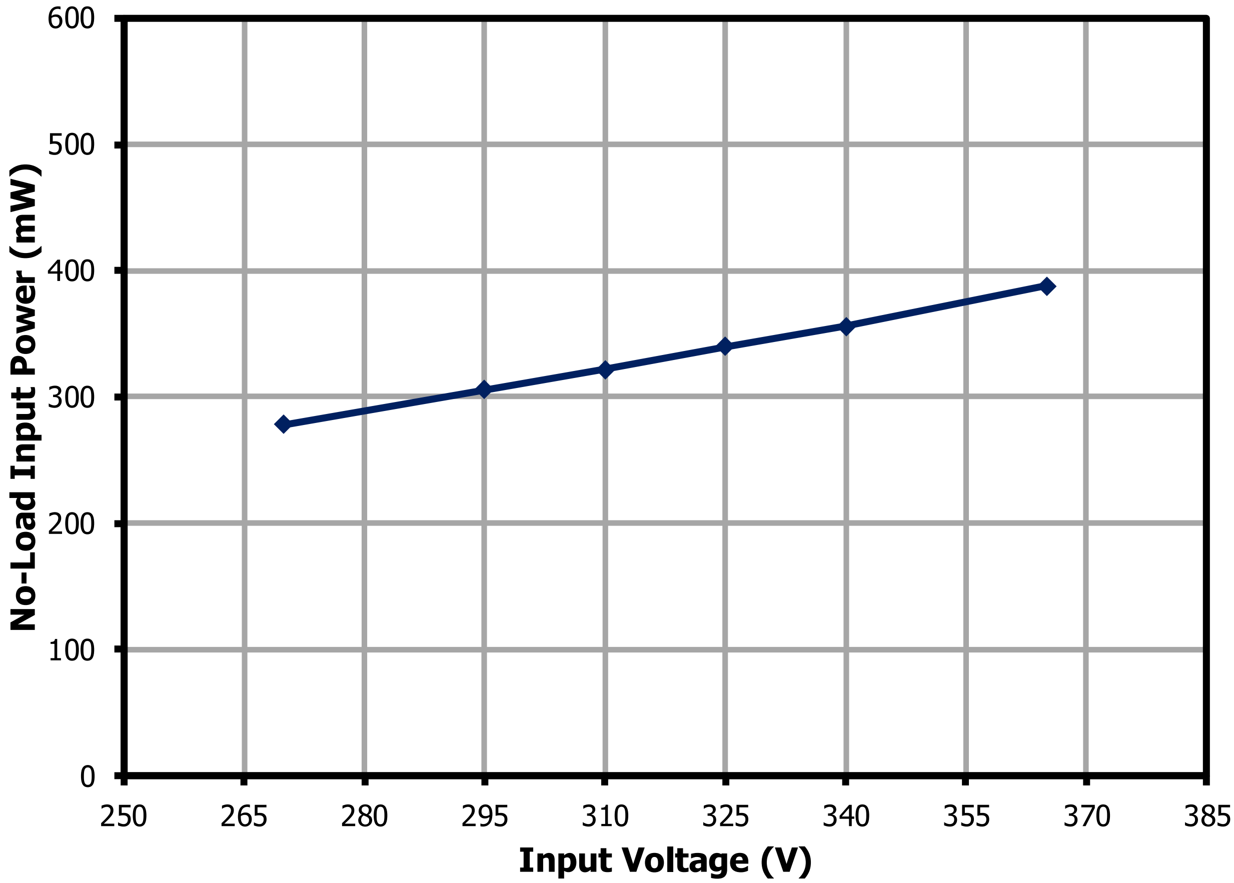

Figure 19 – No-Load Input Power.

7.5 Efficiency

Figure 20 depicts inverter efficiency at 340 V input with 12 kHz high-side PWM frequency and a constant motor speed of 5000 RPM throughout the load range. Table 1 shows the data from the efficiency graph described.

Input DC Voltage (V)	Input DC Current (A)	DC Input Power (W)	Motor RMS Current Phase U (A)	Motor RMS Current Phase V (A)	Motor RMS Current Phase W (A)	Inverter Output Power (W)	Inverter Efficiency (%)
342	0.10	28.64	0.10	0.09	0.10	27.40	95.7
342	0.16	52.10	0.17	0.17	0.18	50.66	97.2
342	0.32	104.12	0.34	0.34	0.35	102.15	98.1
342	0.48	154.99	0.50	0.50	0.51	152.37	98.3
342	0.63	202.81	0.66	0.64	0.67	199.37	98.3
342	0.80	252.55	0.82	0.80	0.83	248.04	98.2
340	0.96	304.54	0.97	0.95	0.99	299.01	98.2

Table 1 – Efficiency.

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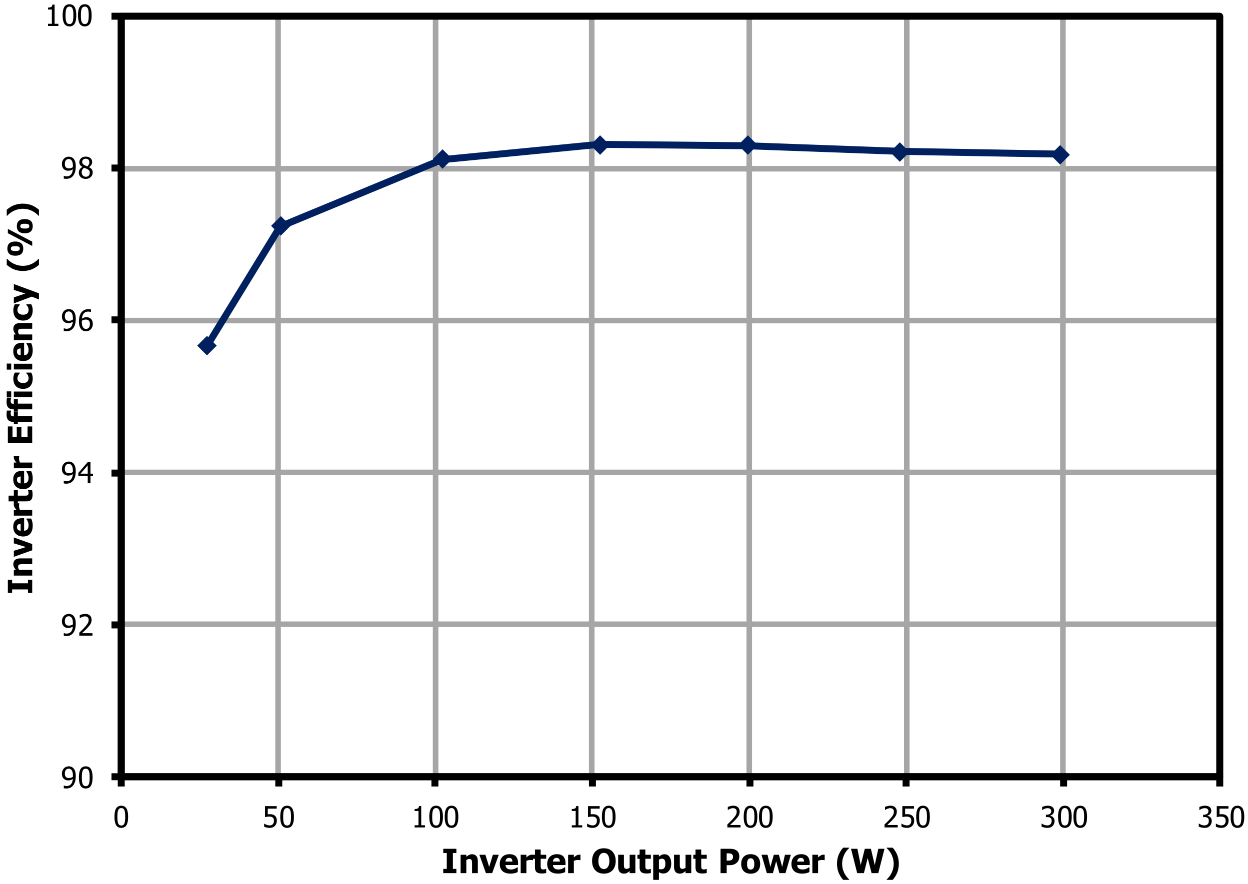

Figure 20 – Inverter Efficiency.

7.6 Device and System Level Protection and Monitoring

This section demonstrates the device integrated and system-level protection and monitoring feature. The device communicates its status update including device or system level fault through the FAULT bus. Each device status word consists of device ID arbitration followed by a 7-bit word pattern and a parity bit. Refer to section 8.2 for the status word encoding summary.

7.6.1 *Device Level Protection*

Figure 21 and Figure 22 depict the integrated current limit function at device U3 (phase W) and associated status update reported on the FAULT bus.

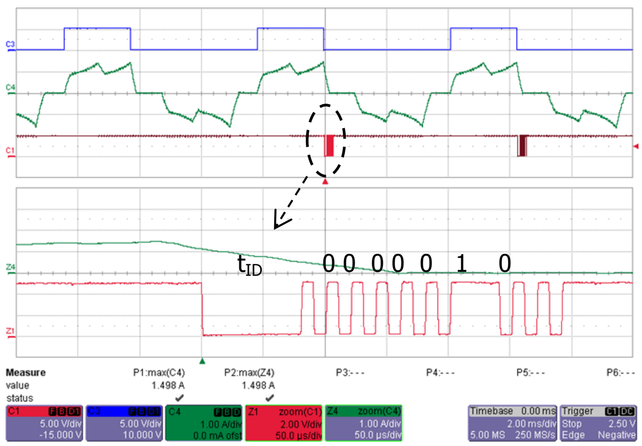

Figure 21 – Over-current - Motor Overload.
Peak Motor Current: 1.49 A R_{XL}: 90 kΩ.
Status Update: 000 00 1 0 (LS OC).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 1 A / div.
Lower: V_{FAULT}, 2 V / div., 2 ms / div.
Zoom: 50 µs / div.

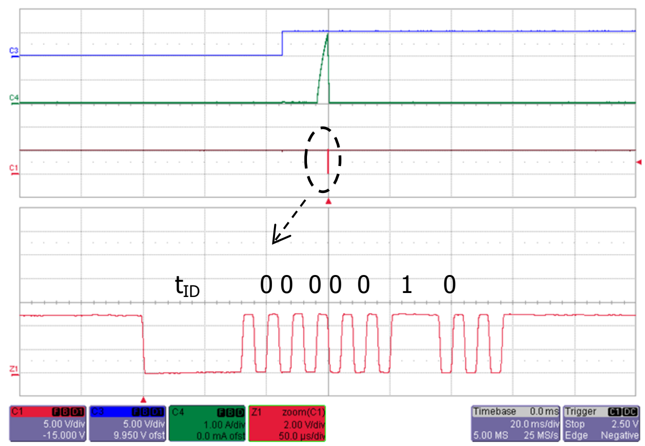

Figure 22 – Over-current - Start-up Stalled Motor.
Peak Motor Current: 3.0 A R_{XL}: 44.2 kΩ.
Status Update: 000 00 1 0 (LS OC)
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 1 A / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

In Figure 21, the current limit resistor R_{XL} was increased to 90 kΩ for test purposes. This sets the overcurrent limit of the Phase W device low-side FREDFET to 1.5 A.

In Figure 22, the current limit resistor R_{XL} of 44.2 kΩ sets the default current limit of 3 A.

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Figure 23 and 24 depict the low-side FREDFET over-temperature warning (OTW) and shutdown (OTS) function and the associated status update reported on the FAULT bus. A localized external heat source applied to the device package forced the temperature rise.

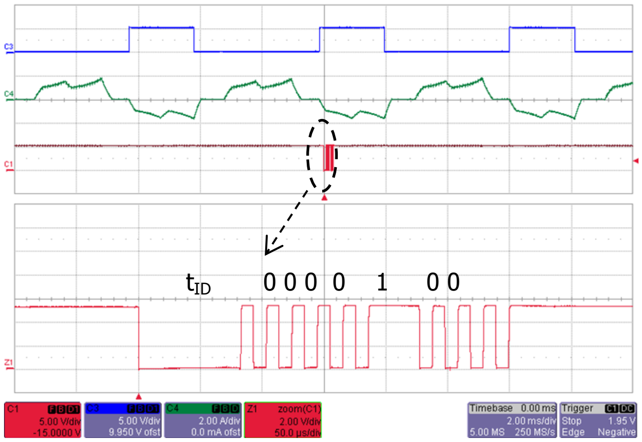

Figure 23 – Temperature Warning, Phase W.
Status Update: 000 01 0 0 (OTW).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 2 A / div.
Lower: V_{FAULT}, 2 V / div., 2 ms / div.
Zoom: 50 μs / div.

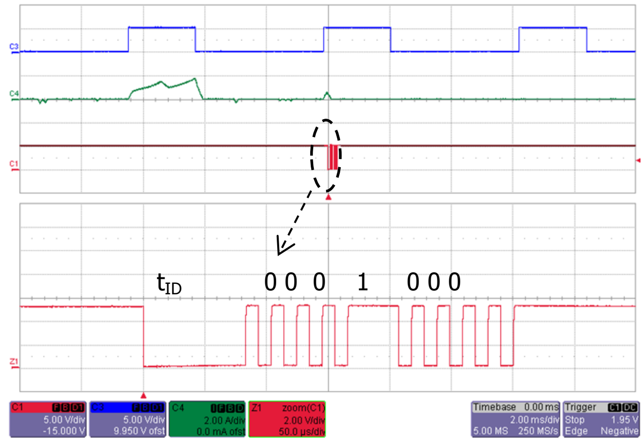

Figure 24 – Thermal Shutdown, Phase W.
Status Update: 000 10 0 0 (OTS).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 2 A / div.
Lower: V_{FAULT}, 2 V / div., 2 ms / div.
Zoom: 50 μs / div.

Figure 25 depicts the status query command (fault bus pulled low for 160 µs) after a thermal shutdown had occurred on the phase W device with the device still under thermal shutdown condition.

Figure 26 shows the status update of phase W device under thermal shutdown.

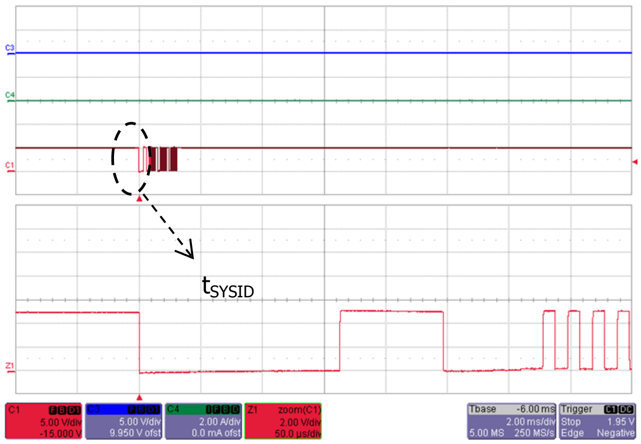

Figure 25 – Status Query.
t_{SYSID}: 160 µs.
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 2 A / div.
Lower: V_{FAULT}, 5 V / div., 2 ms / div.
Zoom: 50 µs / div.

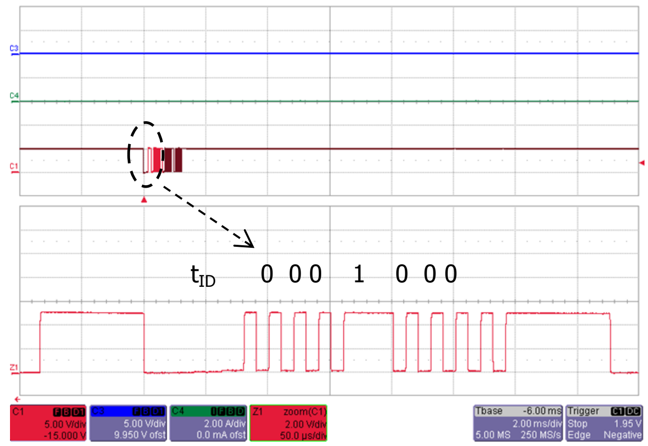

Figure 26 – Status Update, Phase W.
Status Update: 000 10 0 0 (OTS).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 2 A / div.
Lower: V_{FAULT}, 5 V / div., 2 ms / div.
Zoom: 50 µs / div.

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Figure 27 depicts the fault reset command (fault bus pulled low for 2xt_{SS}, 320 µs) to reset the latched thermal shutdown protection on the Phase W device.

Figure 28 depicts the motor restart operation after the fault reset command from the system MCU. The first and second status update corresponds to a device ready status on Phase U and Phase V.

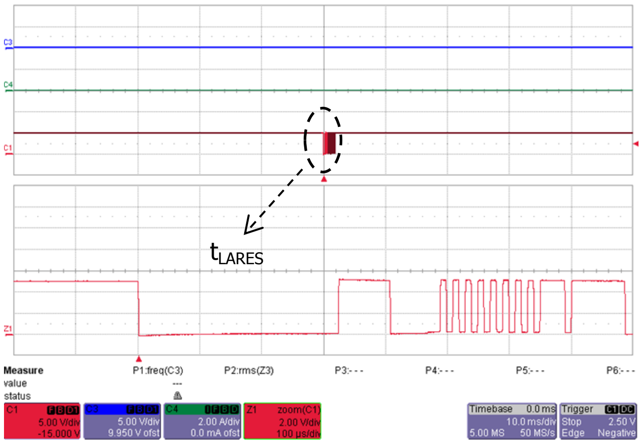

Figure 27 – Fault Reset Command.
t_{LARES}: 320 µs.
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 2 A / div.
Lower: V_{FAULT}, 2 V / div., 10 ms / div.
Zoom: 100 µs / div.

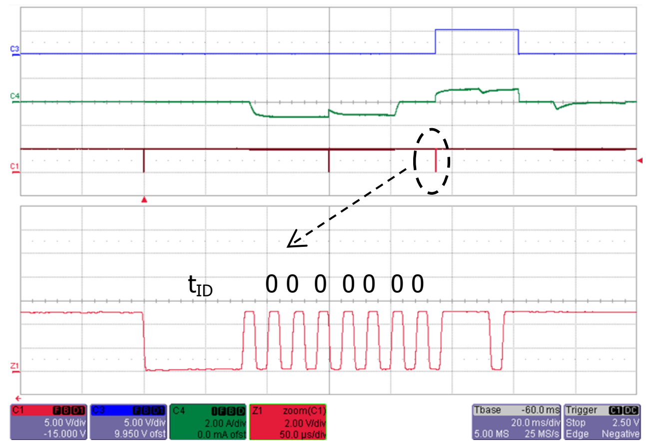

Figure 28 – Status Update, Phase W.
Status Update: 000 00 0 0 (Ready).
Upper: INL Input, 5 V / div.
Middle: $I_{PHASE\ W}$, 2 A / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

7.6.2 *System Level Monitoring*

The test results shown in Figures 29 to 32 demonstrate the integrated HV bus UV monitoring function and status reporting through the communication bus (FAULT pin). Device U1 (Phase U) senses the bus. Its t_{ID} = 40 µs. The input voltage slew rate for all bus monitoring tests is 2 V / ms.

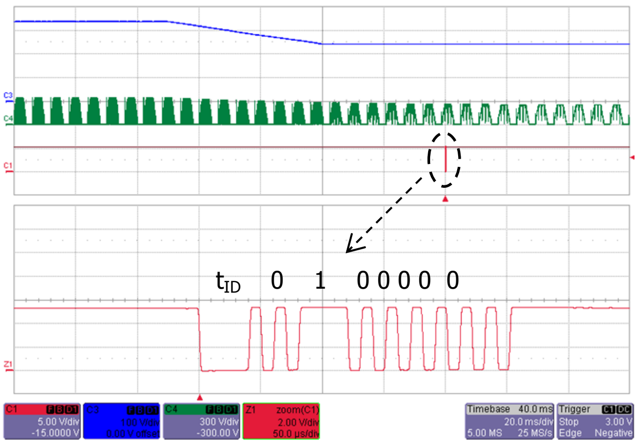

Figure 29 – Bus Sensing - Brown-out.
Bus Voltage Drop 340 to 240 VDC.
Status Update: 010 00 0 0 (UV100).
Upper: V_{BUS}, 100 V / div.
Middle: V_{HB}, 300 V / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

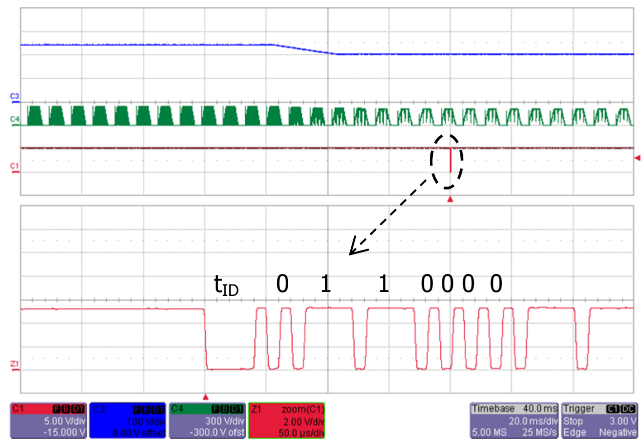

Figure 30 – Bus Sensing - Brown-out.
Bus Voltage Drop 240 to 200 VDC.
Status Update: 011 00 0 0 (UV85).
Upper: V_{BUS}, 100 V / div.
Middle: V_{HB}, 300 V / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

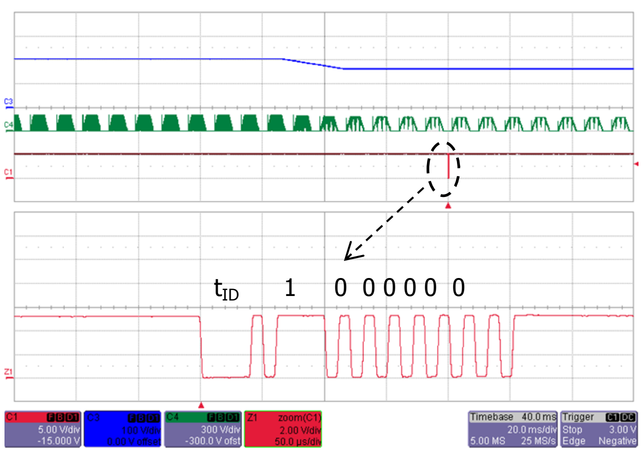

Figure 31 – Bus Sensing - Brown-out.
Bus Voltage Drop 200 to 160 VDC.
Status Update: 100 00 0 0 (UV70).
Upper: V_{BUS}, 100 V / div.
Middle: V_{HB}, 300 V / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

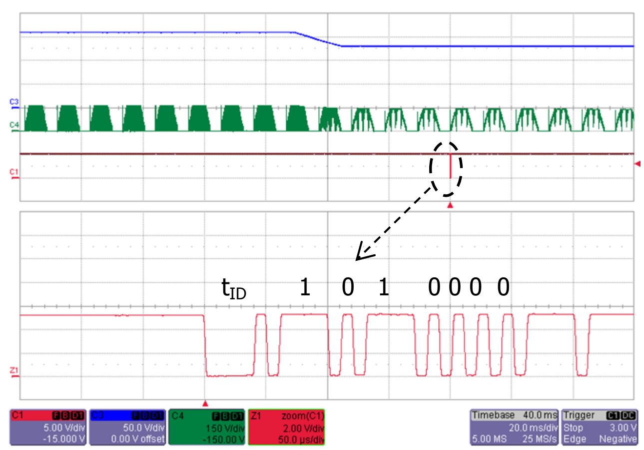

Figure 32 – Bus Sensing - Brown-out.
Bus Voltage Drop 160 to 130 VDC.
Status Update: 101 00 0 0 (UV55).
Upper: V_{BUS}, 50 V / div.
Middle: V_{HB}, 150 V / div.
Lower: V_{FAULT}, 2 V / div., 20 ms / div.
Zoom: 50 µs / div.

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Figure 33 and Figure 34 illustrate the HV bus OV monitoring feature. Device U1 (Phase U) stops switching and reports the OV fault condition as soon as the bus voltage exceeds the set OV threshold (422 V with 7 MΩ). Switching resumes after the bus voltage level drops again below the detection threshold minus the hysteresis (33 V with 7 MΩ).

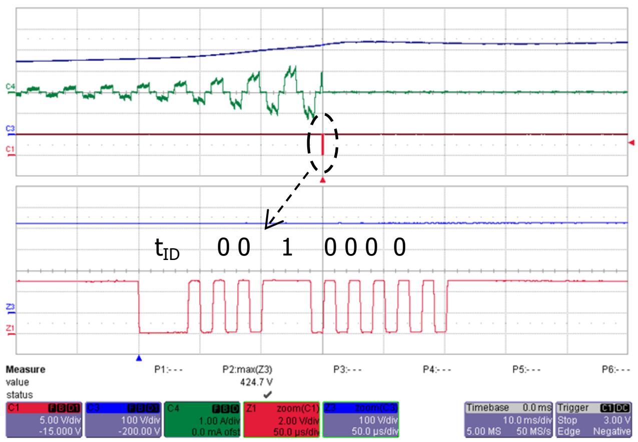

Figure 33 – Bus Sensing - OV Threshold Fault.
Bus Voltage Rise 340 to 430 VDC.
Status Update: 001 00 0 0 (OV).
Upper: V_{BUS}, 100 V / div.
Middle: $I_{PHASE\ U}$, 1 A / div.
Lower: V_{FAULT}, 2 / div., 10 ms / div.
Zoom: 50 µs / div.

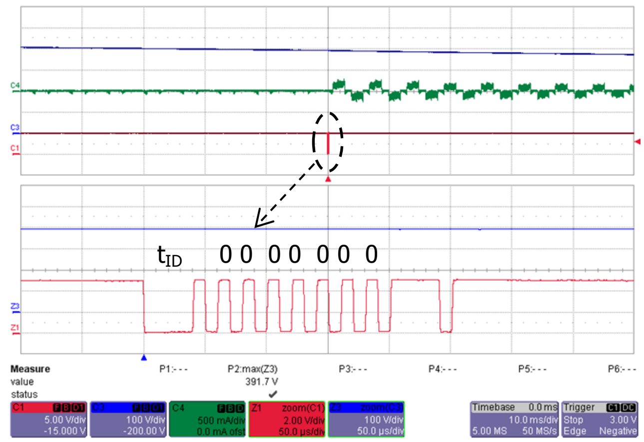

Figure 34 – Bus Sensing - OV Threshold Cleared.
Bus Voltage Drop 430 to 340 VDC.
Status Update: 000 00 0 0 (OV Cleared).
Upper: V_{BUS}, 100 V / div.
Middle: $I_{PHASE\ U}$, 500 mA / div.
Lower: V_{FAULT}, 2 / div., 10 ms / div.
Zoom: 50 µs / div.

Figure 35 and Figure 36 illustrate the system-level temperature monitoring function. The device checks the resistance connected to the SM pin every second for a period of 10 ms.

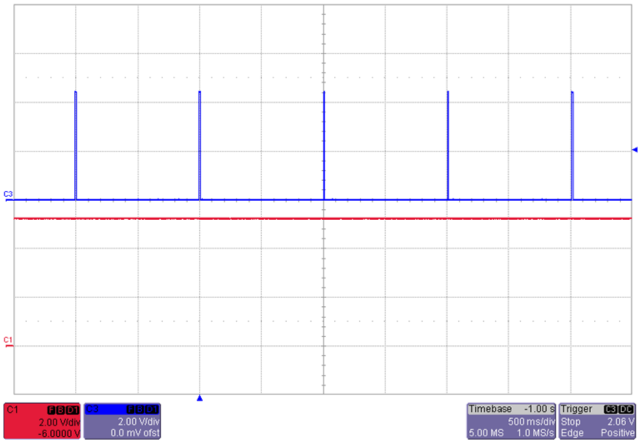

Figure 35 – External Temperature Sensing.
Sense Pulse Repetition rate: 1 Hz.
Sense Pulse Duration: 10 ms.
Upper: V_{SM}, 2 V / div.
Lower: V_{FAULT}, 2 V / div., 500 ms / div.

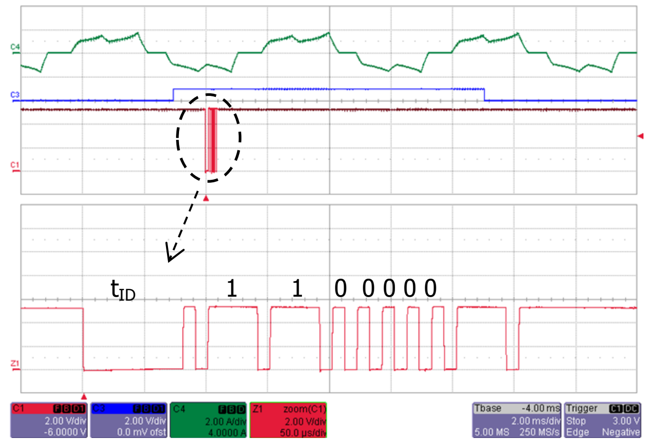

Figure 36 – External Temperature Fault Detected.
Status Update: 110 00 0 0 (System OT).
Upper: $I_{PHASE\ W}$, 2 A / div.
Middle: V_{SM}, 2 V / div.
Lower: V_{FAULT}, 2 V / div., 2 ms / div.
Zoom: 50 μs / div.

The fault was simulated by applying a localized external heat gun to sense thermistor RT2.

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7.6.3 *Status Query*

Figure 37 to Figure 40 illustrate a status query sequence initiated from the system MCU by pulling the status bus low for t_{SYSID}. The DC bus voltage was set to 240 VDC for this illustration. Consequently, the device U1 (Phase U) which monitors the bus voltage, reports a UV100 condition during its status update as shown in Figure 38. The two other devices report an all clear during their respective status update.

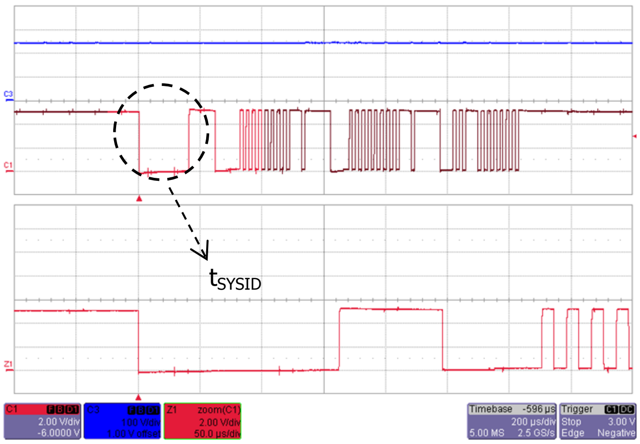

Figure 37 – Status Query - System MCU Request.
Request Time t_{SYSID}: 160 µs.
Upper: V_{BUS}, 100 V / div.
Lower: V_{FAULT}, 2 V / div., 200 µs / div.
Zoom: 50 µs / div.

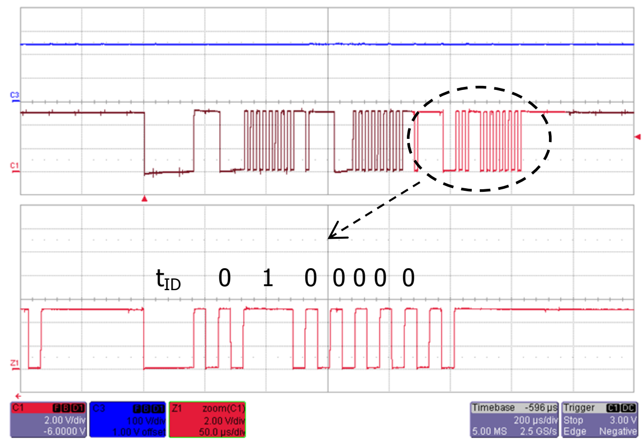

Figure 38 – Status Query - Device ID 1 Response, Phase U.
Status Update: 010 00 0 0 (UV100).
Upper: V_{BUS}, 100 V / div.
Lower: V_{FAULT}, 2 V / div., 200 µs / div.
Zoom: 50 µs / div.

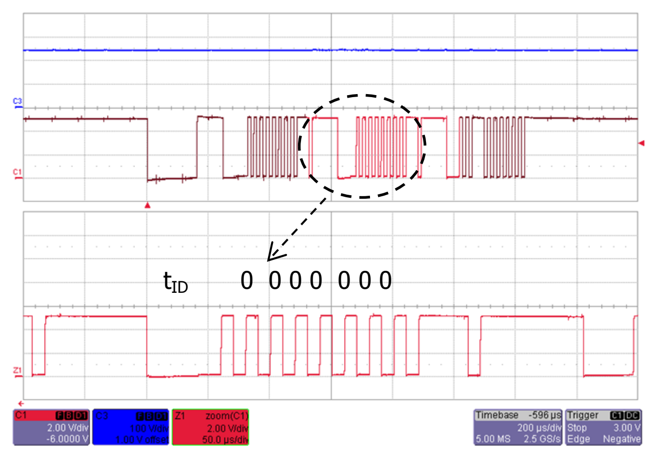

Figure 39 – Status Query - Device ID 2 Response, Phase V.
Status Update: 000 00 0 0 (clear)
Upper: V_{BUS}, 100 V / div.
Lower: V_{FAULT}, 2 V / div., 200 µs / div.
Zoom: 50 µs / div.

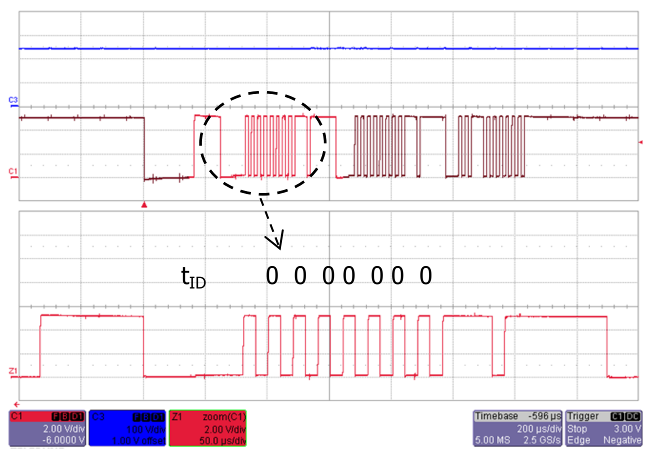

Figure 40 – Status Query - Device ID 3 Response, Phase W.
Status Update: 000 00 0 0 (clear)
Upper: V_{BUS}, 100 V / div.
Lower: V_{FAULT}, 2 V / div., 200 µs / div.
Zoom: 50 µs / div.

7.7 Abnormal Motor Operation Tests

This paragraph provides results during abnormal operation tests for appliances with motors as described in IEC 60335-1 (Safety of household and similar electrical appliances). The tests include:

- Operation under stalled motor conditions
- Operation with one motor winding disconnected
- Running overload test

The test results demonstrate the integrated protection features of the BridgeSwitch under such abnormal operations. The motor operates at 300 W and 5000 RPM at 340 Vdc rated voltage for all test cases except for the overload test.

7.7.1 *Operation Under Stalled (Motor) Conditions*

Figure 41 and Figure 42 depict the motor phase currents and overcurrent fault flag on Phase V when doing startup with a motor stalled condition. The inverter is continuously supplied for a period of 10 minutes at the rated voltage at this condition. The motor is non-operational with no device or motor damage during or after this test.

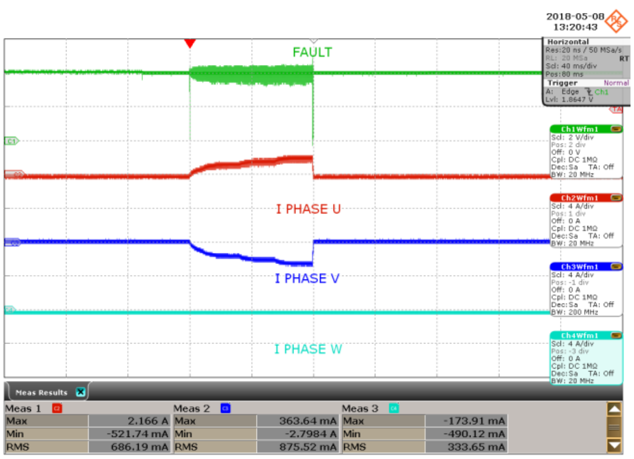

Figure 41 – Motor Stalled at Start-up Condition.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div. 40 ms / div.

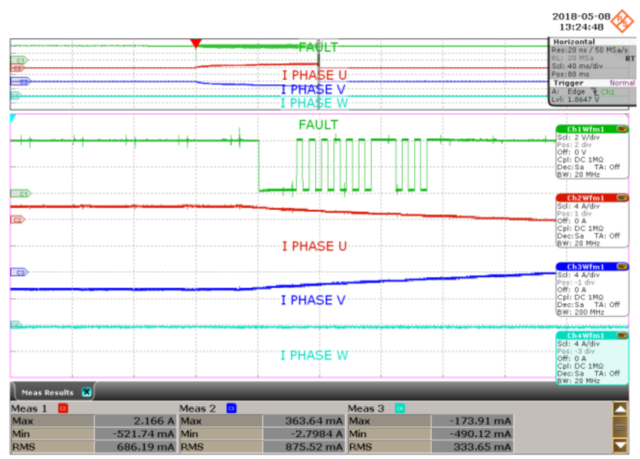

Figure 42 – Fault Flag: 000 00 1 0.
Low-side Overcurrent, Phase V.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div., 40 ms / div.
Zoom: 1 ms / div.

Figure 43 and 44 depict the motor phase currents and fault flags when the motor is stalled during running operation. The inverter is continuously supplied for a period of 10 minutes at the rated voltage at this condition. BridgeSwitch reports over-current fault conditions, and the motor is non-operational with no device or motor damage during the test or after the fault is removed.

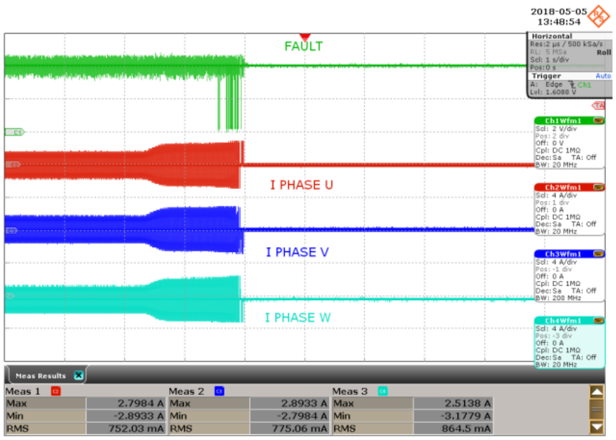

Figure 43 – Motor Stalled at Running Condition.
Multiple Overcurrent Flags Reported.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div. 1 s / div.

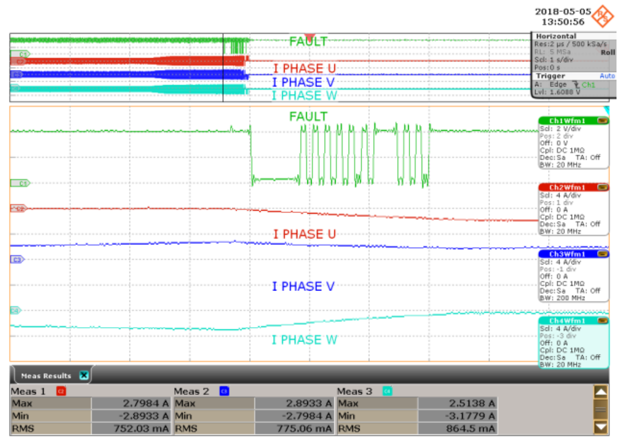

Figure 44 – First Fault Flag: 000 00 1 0.
Low-side overcurrent, Phase W.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div., 1 s / div.
Zoom: 1 ms / div.

7.7.2 *Operation with One Motor Winding Disconnected*

Figure 45 and 46 depict the motor phase currents and fault flag during operation with one motor winding disconnected.

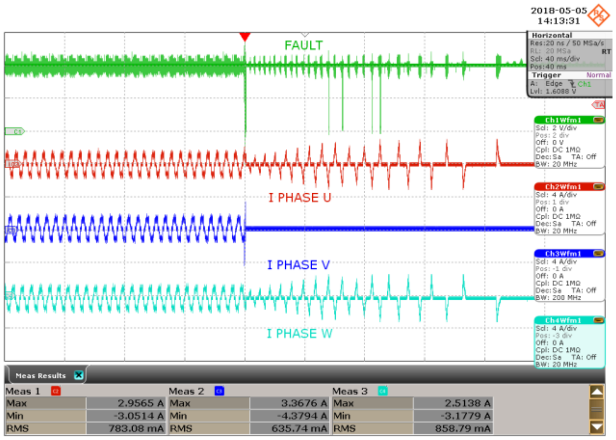

Figure 45 – Phase V Winding Disconnected.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div., 40 ms / div.

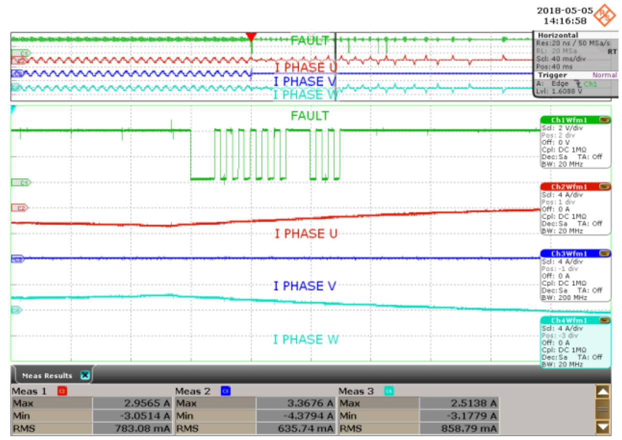

Figure 46 – Fault Flag: 000 00 1 0.
Low-side Overcurrent, Phase U.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div., 40 ms / div.
Zoom: 1 ms / div.

The device reports overcurrent status updates and the motor operates abnormally before completely stalling with no device or motor damage.

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7.7.3 *Running Overload Test*

Figure 47 and Figure 48 depict the motor phase currents and status update flag during a running overload fault condition. During this test, the motor load is increased such that the current through the motor windings increases by 10% and until steady conditions are established. The load is then increased again and the test repeats until the BridgeSwitch protection engages or the motor stalls.

With the motor stalled condition, the inverter is supplied continuously for a period of 10 minutes at the rated voltage. Every device reports status updates and the motor is non-operational with no device or motor damage.

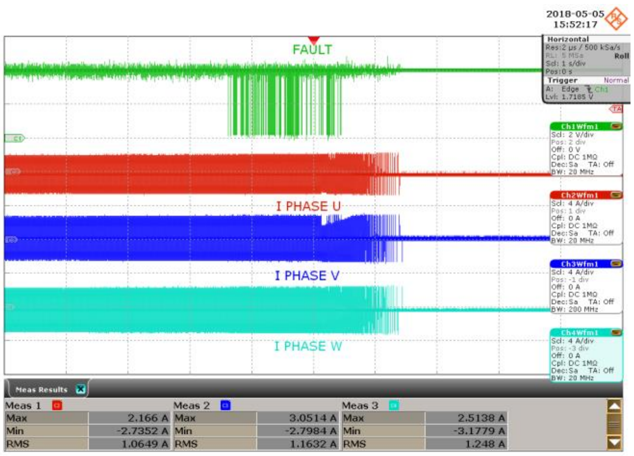

Figure 47 – Running Overload Test >450 W.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div., 1 s / div.

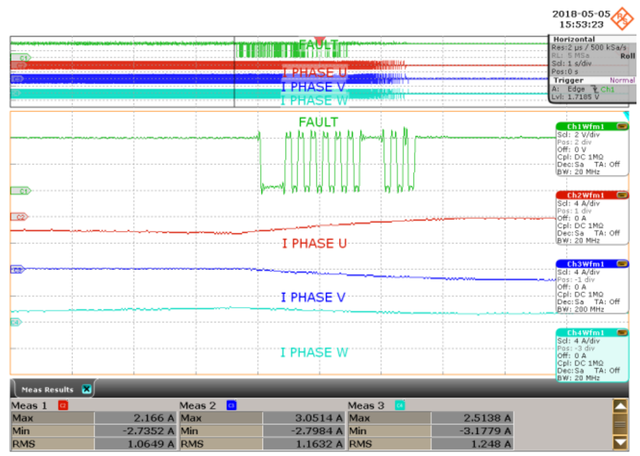

Figure 48 – First Fault Flag: 000 00 1 0.
Low-side Overcurrent, Phase U.
First: V_{FAULT}, 2 V / div.
Second: $I_{PHASE\ U}$, 4 A / div.
Third: $I_{PHASE\ V}$, 4 A / div.
Fourth: $I_{PHASE\ W}$, 4 A / div., 1 s / div.
Zoom: 1 ms / div.

8 Appendix

8.1 Inverter Circuit Board Manual

8.1.1 *Connectors*

Figure 49 shows locations and functions of all connectors to and from a test system.

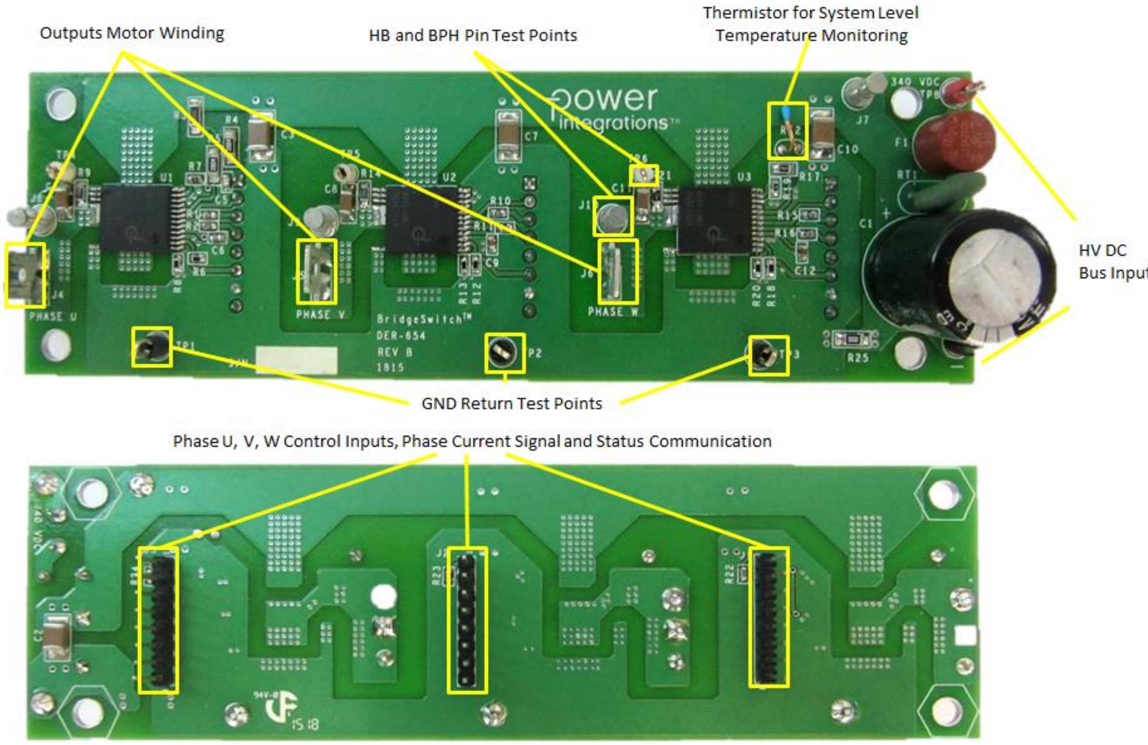

Figure 49 – Test Platform Connections (Top and Bottom View).

The high-voltage DC bus connects to the inverter through two through-hole mount test points, J7 and J8. The positive input terminal should connect to J8, and the negative input terminal should connect to J7.

Control input signals and a system monitor and communication output signals connect to the test system through three 8-position header breakaway connectors J1, J2, and J3 (Figure 50). Figure 50 depicts physical dimensions and pin numbers.

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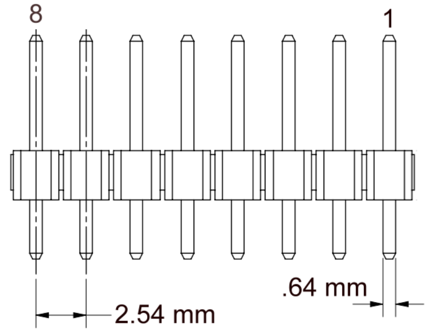

Figure 50 – Control Input and System Monitor Output Connectors (J1, J2, J3).

Table 2 lists all input and output signals on each of the three connectors for control input, phase current signal and status communication output.

Pin No.	Signal	Type	Comments
1	VDDx	Input	Pull-up supply for communication bus, 3.3 V ±5% or 5 V ±5% compatible
2	FAULT_x	Input/Output	Single wire, bi-directional communication bus (open-Drain architecture)
3	PWMxH	Input	Gate drive signal for high-side power FREDFET, active low, 3.3 V or 5 V CMOS compatible
4	PWMxL	Input	Gate drive signal for low-side power FREDFET, active high, 3.3 V or 5 V CMOS compatible
5	NC	n/a	No connection
6	IPH_x	Output	Voltage signal proportional to instantaneous phase low-side FREDFET Drain current, 1 V per 1 A Drain current signal ratio
7	Ground	n/a	Reference for connector input and output signals and system microcontroller
8	NC	n/a	No connection

Table 2 – Control Input, Phase Current Signal, and Status Communication Output Connector Pinout.

The three motor winding outputs connect to the inverter through quick mount terminals as shown in Figure 51.

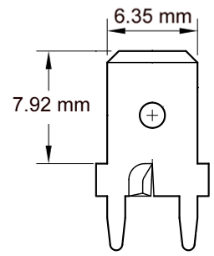

Figure 51 – Quick Mount Terminals for Motor Outputs (J4, J5, and J6).

8.1.2 *Test Points*

The design example board offers various signal test points to support the evaluation. Table 3 lists the available test points and the respective probed signals.

Test Point	Probed Signal
Inverter	
TP8	HV DC bus positive input
TP4	HV DC bus negative input
J7	HV DC bus positive test point
Phase U	
J8	Half-bridge voltage
TP4	Device high-side supply voltage
TP1	System ground
Phase V	
J9	Half-bridge voltage
TP5	Device high-side supply voltage
TP2	System ground
Phase W	
J10	Half-bridge voltage
TP6	Device high-side supply voltage
TP3	System ground

Table 3 – Test Points.

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8.1.3 *Recommended Start-up Sequence*

BridgeSwitch devices have internal self-supply supporting commutation PWM frequencies up to 20 kHz. To ensure sufficient supply voltage levels across the BPL pin capacitor and the BPH pin capacitor at inverter startup, the system microcontroller (MCU) should follow the recommended power-up sequence depicted in Figure 52.

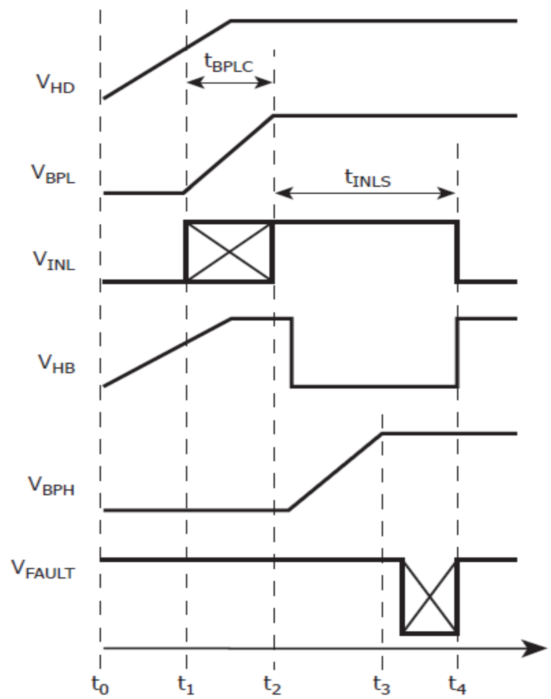

Figure 52 – Recommended Power-up Sequence with Self-Supplied Operation.

Table 4 lists activities occurring during the recommended the power-up sequence.

Time Point	Activity
t_0	• High-voltage DC bus is applied
t_1	• Internal current source starts charging BPL pin capacitor once HD-pin voltage reaches $V_{HD(START)}$ • System MCU may start setting low-side power-FREDFET control signal INL to high
t_2	• BPL pin voltage reaches V_{BPL} (typ. 14.5 V) • Device determines external device settings • Internal Gate drive logic turns on low-side power FREDFET after device setup completes and once INL becomes high or if it is high already • Internal current source charges BPH pin capacitor
t_3	• BPH pin voltage reaches V_{BPH} with respect to HB pin (typically 14.5 V) • Device starts communicating successful power-up through fault pin Note: The device does not send a status update if the internal power-up sequence did not complete successfully
t_4	• BridgeSwitch is ready for state operation (indicated by communicated status update at time point t_3) • System MCU turns off low-side FREDFET

Table 4 – Power-up Sequence with Self-Supplied Operation.

8.2 Status Word Encoding

Figure 53 depicts the status word encoding summary of various device status including device or system-level faults demonstrated in section 7.6.

Status	Parameter	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6
High-voltage bus OV	I_{OV}	0	0	1	X	X	X	X
High-voltage bus UV 100%	I_{UV100}	0	1	0	X	X	X	X
High-voltage bus UV 85%	I_{UV85}	0	1	1	X	X	X	X
High-voltage bus UV 70%	I_{UV70}	1	0	0	X	X	X	X
High-voltage bus UV 55%	I_{UV55}	1	0	1	X	X	X	X
System thermal fault	$V_{TH(TM)}$	1	1	0	X	X	X	X
LS Driver not ready[1]	n/a	1	1	1	X	X	X	X
LS FET thermal warning	T_{WA}	X	X	X	0	1	X	X
LS FET thermal shutdown	T_{SD}	X	X	X	1	0	X	X
HS Driver not ready[2]	I_{COM}	X	X	X	1	1	X	X
LS FET over-current	$V_{X(TH)}$	X	X	X	X	X	1	X
HS FET over-current	$V_{X(TH)}$	X	X	X	X	X	X	1
Device Ready (no faults)	n/a	0	0	0	0	0	0	0

Notes:
1. Includes XL pin open/short-circuit fault and IPH pin to XL pin short-circuit.
2. Includes internal communication loss, supply out of range, and XH pin open/short-circuit fault.

Figure 53 – Status Word Encoding.

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8.3 Test Bench Set-up

Figure 54 depicts the test bench used to gather the performance data presented in this report. It consists of:

- 3-phase inverter using BRD1265C with interface board for MCU and hall sensor interface
- Cypress CY8CKIT-042 PSOC4 MCU motor control unit (not visible)
  - Trapezoidal control with 12 kHz high-side PWM
- Shunde Hopemotion brushless DC motor 57BL110S30-3150TFO
  - 310 VDC, 5000 RPM, 0.7 Nm, 300 W, 4 poles, hall sensor outputs
- Dongguan ZL Electromechanics hysteresis brake including control unit
- Programmable DC input source Chroma Model 61502 (not shown)
- Bench power supply for MCU control board and motor brake controller

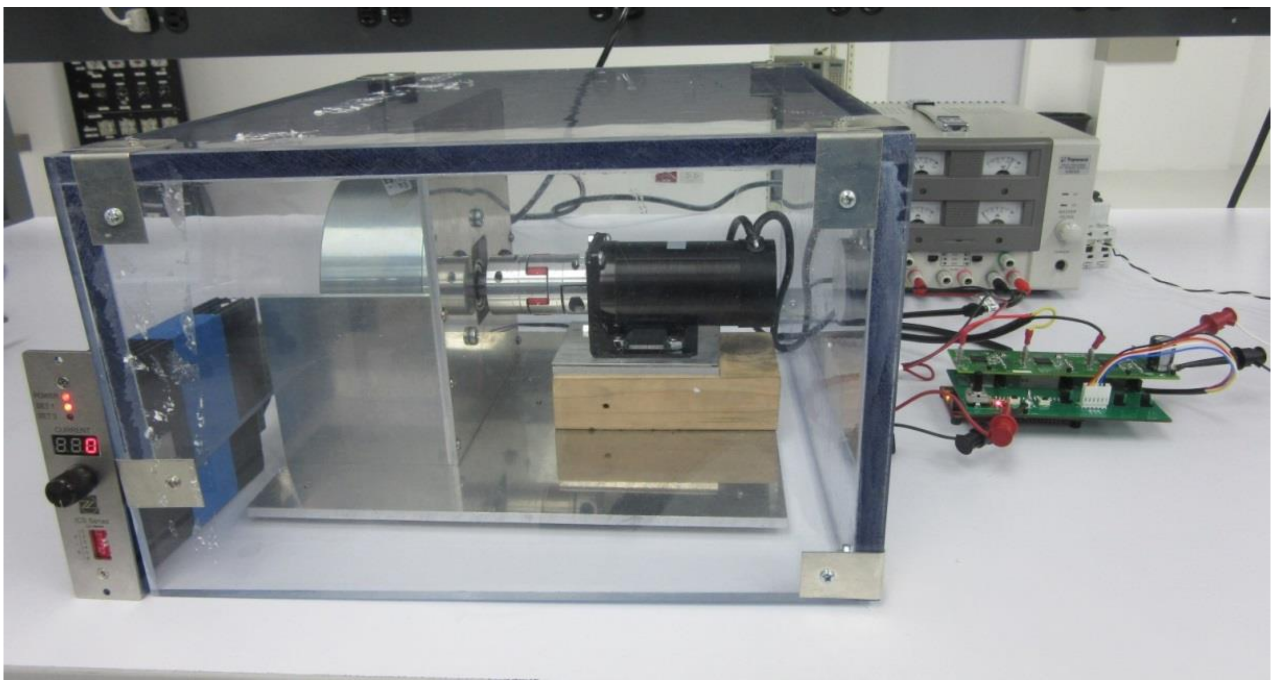

Figure 54 – Test Bench Set-up.

8.4 Inverter Output Power Measurement

3-phase inverter output power P_{OUT} and efficiency measurements apply the "two wattmeter" method illustrated in Figure 55 below.

$$P_{OUT} = P_{CH1} + P_{CH2}$$

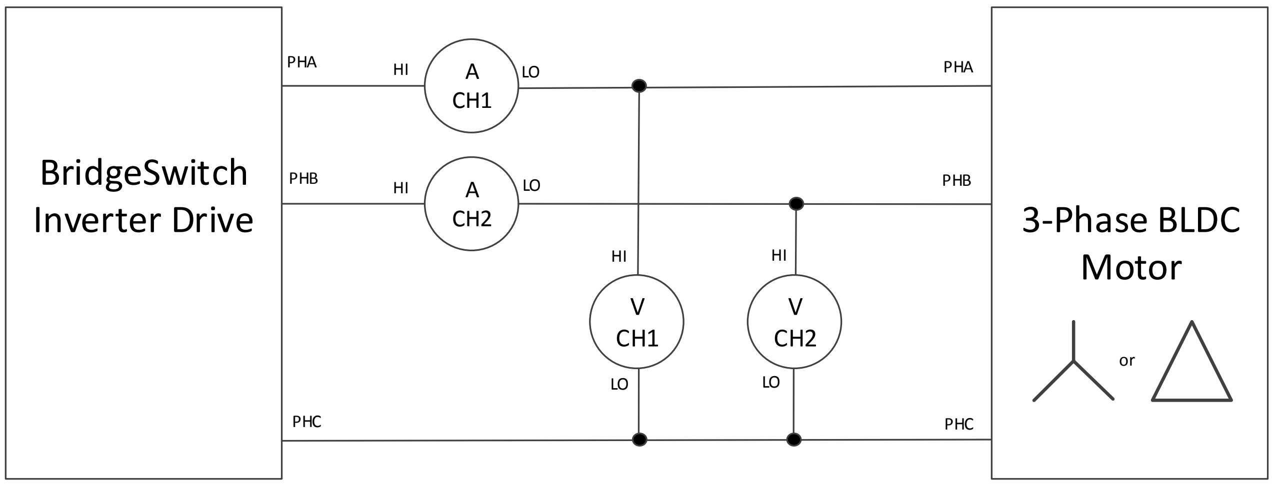

Figure 55 – Inverter Output Power Measurement.

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9 Notes

Described below are the oscilloscope model and settings used to gather the waveform plots presented in the performance data section of this document:

- In section 7.1 (Start-up operation) up to section 7.6 (Device and system level protection): 6050A Lecroy 500 MHz oscilloscope set to 20 MHz Bandwidth with 3-bit resolution enhancement.
- In section 7.7 (Motor abnormal tests): RTO2004 Rhode & Schwarz 600 MHz oscilloscope set to 20 MHz bandwidth.

10 Revision History

Date	Author	Revision	Description & Changes	Reviewed
02-Oct-18	JHP	1.0	Initial Release.	Apps & Mktg
20-May-19	JHP	1.1	Updated Notes in Section 2.	Apps & Mktg

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